CMOS 300 MSPS Quadrature Complete DDS

AD9854

FEATURES

- 300 MHz internal clock rate
- FSK, BPSK, PSK, CHIRP, AM operation
- Dual integrated 12-bit D/A converters
- Ultrahigh speed comparator, 3 ps rms jitter
- Excellent dynamic performance:
  - 80 dB SFDR @ 100 MHz (±1 MHz) A_{OUT}
- 4× to 20× programmable reference clock multiplier
- Dual 48-bit programmable frequency registers
- Dual 14-bit programmable phase offset registers
- 12-bit amplitude modulation and programmable shaped on/off keying function
- Single-pin FSK and BPSK data interface
- PSK capability via I/O interface
- Linear or nonlinear FM chirp functions with single-pin frequency hold function
- Frequency-ramped FSK
- < 25 ps rms total jitter in clock generator mode
- Automatic bidirectional frequency sweeping
- SIN(x)/x correction
- Simplified control interfaces:
  - 10 MHz serial, 2-wire or 3-wire SPI®-compatible
  - 100 MHz parallel 8-bit programming
- 3.3 V single supply
- Multiple power-down functions
- Single-ended or differential input reference clock
- Small 80-lead LQFP packaging

APPLICATIONS

- Agile, quadrature LO frequency synthesis
- Programmable clock generators
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Commercial and amateur RF exciters

FUNCTIONAL BLOCK DIAGRAM

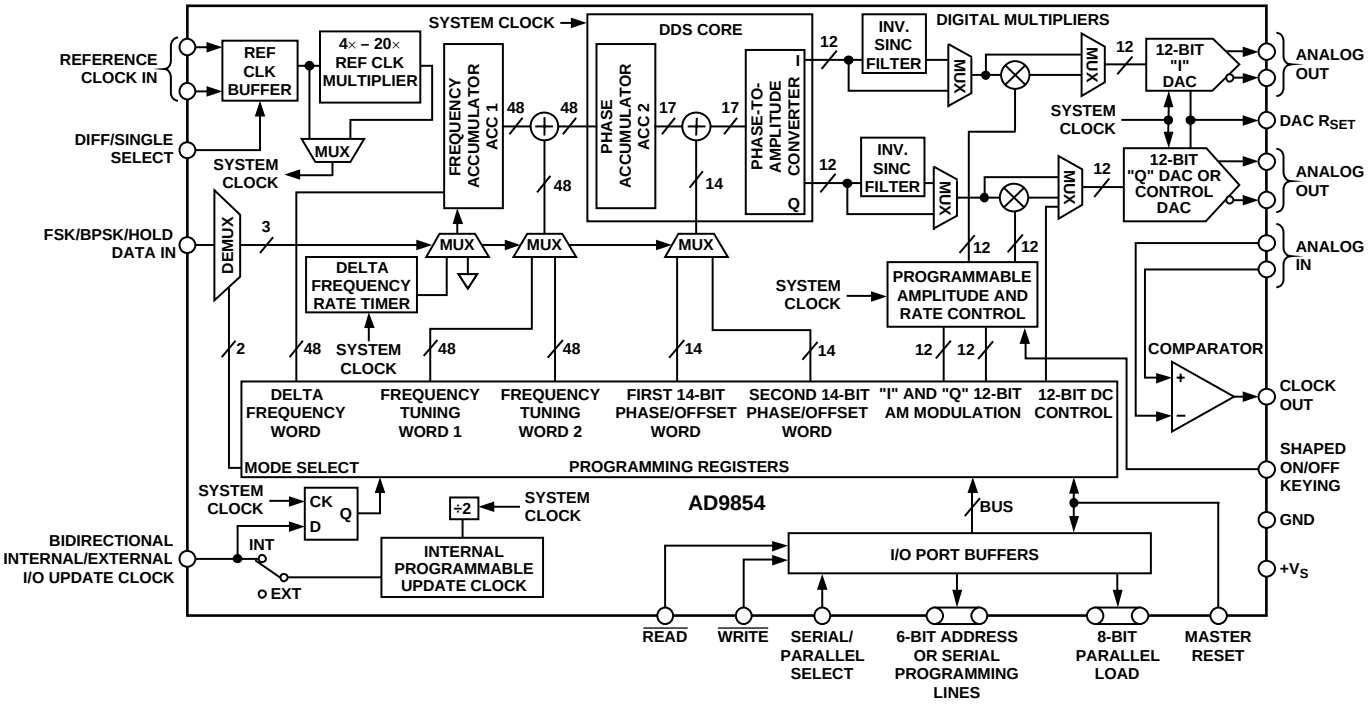

Figure 1.

Rev. C

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GENERAL DESCRIPTION

The AD9854 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with two internal high speed, high performance quadrature D/A converters to form a digitally programmable I and Q synthesizer function. When referenced to an accurate clock source, the AD9854 generates highly stable, frequency-phase amplitude-programmable sine and cosine outputs that can be used as an agile LO in communications, radar, and many other applications. The AD9854's innovative high speed DDS core provides 48-bit frequency resolution (1 MHz tuning resolution with 300 MHz SYSCLK). Maintaining 17 bits assures excellent SFDR. The AD9854's circuit architecture allows the generation of simultaneous quadrature output signals at frequencies up to 150 MHz, which can be digitally tuned at a rate of up to 100 million new frequencies per second. The sine wave output (externally filtered) can be converted to a square wave by the internal comparator for agile clock generator applications. The device provides two 14-bit phase registers and a single pin for BPSK operation. For higher-order PSK operation, the I/O interface may be used for phase changes. The 12-bit I and Q DACs, coupled with the innovative DDS architecture, provide excellent wideband and narrow-band output SFDR. The Q DAC can also be configured as a user-programmable control DAC if the quadrature function is not desired. When configured with the comparator, the 12-bit control DAC facilitates static duty cycle control in high speed clock generator applications. Two 12-bit digital multipliers permit programmable amplitude modulation, shaped on/off keying, and precise amplitude control of the quadrature output. Chirp functionality is also included to facilitate wide bandwidth frequency sweeping applications. The AD9854's programmable 4× to 20× REFCLK multiplier circuit generates the 300 MHz system clock internally from a lower frequency external reference clock. This saves the user the expense and difficulty of implementing a 300 MHz system clock source. Direct 300 MHz clocking is also accommodated with either single-ended or differential inputs. Single-pin conventional FSK and the enhanced spectral qualities of ramped FSK are supported.The AD9854 uses advanced 0.35 micron CMOS technology to provide a high level of functionality on a single 3.3 V supply.

The AD9854 is available in a space-saving 80-lead LQFP surface-mount package and a thermally enhanced 80-lead LQFP package. The AD9854 is pin-for-pin compatible with the AD9852 single-tone synthesizer. It is specified to operate over the extended industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

V_S = 3.3 V ± 5%, R_{SET} = 3.9 kΩ, external reference clock frequency = 30 MHz with REFCLK multiplier enabled at 10× for AD9854ASQ, external reference clock frequency = 20 MHz with REFCLK multiplier enabled at 10× for AD9854AST, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	AD9854ASQ			AD9854AST			Unit
			Min	Typ	Max	Min	Typ	Max	
REF CLOCK INPUT CHARACTERISTICS[1]									
Internal System Clock Frequency Range									
REFCLK Multiplier Enabled	Full	VI	20		300	20		200	MHz
REFCLK Multiplier Disabled	Full	VI	DC		300	DC		200	MHz
External REF Clock Frequency Range									
REFCLK Multiplier Enabled	Full	VI	5		75	5		50	MHz
REFCLK Multiplier Disabled	Full	VI	DC		300	DC		200	MHz
Duty Cycle	25°C	IV	45	50	55	45	50	55	%
Input Capacitance	25°C	IV		3			3		pF
Input Impedance	25°C	IV		100			100		kΩ
Differential Mode Common-Mode Voltage Range									
Minimum Signal Amplitude[2]	25°C	IV	400			400			mV p-p
Common-Mode Range	25°C	IV	1.6	1.75	1.9	1.6	1.75	1.9	V
VIH (Single-Ended Mode)	25°C	IV	2.3			2.3			V
VIL (Single-Ended Mode)	25°C	IV			1			1	V
DAC STATIC OUTPUT CHARACTERISTICS									
Output Update Speed	Full	I			300			200	MSPS
Resolution	25°C	IV		12			12		Bits
I and Q Full-Scale Output Current	25°C	IV	5	10	20	5	10	20	mA
I and Q DAC DC Gain Imbalance[3]	25°C	I	−0.5	+0.15	+0.5	−0.5	+0.15	+0.5	dB
Gain Error	25°C	I	−6		+2.25	−6		+2.25	% FS
Output Offset	25°C	I			2			2	µA
Differential Nonlinearity	25°C	I		0.3	1.25		0.3	1.25	LSB
Integral Nonlinearity	25°C	I		0.6	1.66		0.6	1.66	LSB
Output Impedance	25°C	IV		100			100		kΩ
Voltage Compliance Range	25°C	I	−0.5		+1.0	−0.5		+1.0	V
DAC DYNAMIC OUTPUT CHARACTERISTICS									
I and Q DAC Quad. Phase Error	25°C	IV		0.2	1		0.2	1	Degrees
DAC Wideband SFDR									
1 MHz to 20 MHz A_{OUT}	25°C	V		58			58		dBc
20 MHz to 40 MHz A_{OUT}	25°C	V		56			56		dBc
40 MHz to 60 MHz A_{OUT}	25°C	V		52			52		dBc
60 MHz to 80 MHz A_{OUT}	25°C	V		48			48		dBc
80 MHz to 100 MHz A_{OUT}	25°C	V		48			48		dBc
100 MHz to 120 MHz A_{OUT}	25°C	V		48			48		dBc
DAC Narrow-Band SFDR									
10 MHz A_{OUT}(±1 MHz)	25°C	V		83			83		dBc
10 MHz A_{OUT} (±250 kHz)	25°C	V		83			83		dBc
10 MHz A_{OUT} (±50 kHz)	25°C	V		91			91		dBc
41 MHz A_{OUT} (±1 MHz)	25°C	V		82			82		dBc
41 MHz A_{OUT} (±250 kHz)	25°C	V		84			84		dBc
41 MHz A_{OUT} (±50 kHz)	25°C	V		89			89		dBc
119 MHz A_{OUT} (±1 MHz)	25°C	V		71			71		dBc
119 MHz A_{OUT} (±250 kHz)	25°C	V		77			77		dBc
119 MHz A_{OUT} (±50 kHz)	25°C	V		83			83		dBc

Parameter	Temp	Test Level	AD9854ASQ			AD9854AST			Unit
			Min	Typ	Max	Min	Typ	Max	
Residual Phase Noise									
(A_{OUT} = 5 MHz, Ext. CLK = 30 MHz,									
REFCLK Multiplier Engaged at 10×)									
1 kHz Offset	25°C	V		140			140		dBc/Hz
10 kHz Offset	25°C	V		138			138		dBc/Hz
100 kHz Offset	25°C	V		142			142		dBc/Hz
(A_{OUT} = 5 MHz, Ext. CLK = 300 MHz,									
REFCLK Multiplier Bypassed)									
1 kHz Offset	25°C	V		142			142		dBc/Hz
10 kHz Offset	25°C	V		148			148		dBc/Hz
100 kHz Offset	25°C	V		152			152		dBc/Hz
Pipeline Delays[4, 5, 6]									
DDS Core (Phase Accumulator and Phase-to-Amp Converter)	25°C	IV		33			33		SysClk Cycles
Frequency Accumulator	25°C	IV		26			26		SysClk Cycles
Inverse Sinc Filter	25°C	IV		16			16		SysClk Cycles
Digital Multiplier	25°C	IV		9			9		SysClk Cycles
DAC	25°C	IV		1			1		SysClk Cycles
I/O Update Clock (INT MODE)	25°C	IV		2			2		SysClk Cycles
I/O Update Clock (EXT MODE)	25°C	IV		3			3		SysClk Cycles
MASTER RESET DURATION	25°C	IV	10			10			SysClk Cycles
COMPARATOR INPUT CHARACTERISTICS									
Input Capacitance	25°C	V		3			3		pF
Input Resistance	25°C	IV		500			500		kΩ
Input Current	25°C	I		±1	±5		±1	±5	µA
Hysteresis	25°C	IV		10	20		10	20	mV p-p
COMPARATOR OUTPUT CHARACTERISTICS									
Logic 1 Voltage, High Z Load	Full	VI	3.1			3.1			V
Logic 0 Voltage, High Z Load	Full	VI			0.16			0.16	V
Output Power, 50 Ω Load, 120 MHz Toggle Rate	25°C	I	9	11		9	11		dBm
Propagation Delay	25°C	IV		3			3		ns
Output Duty Cycle Error[7]	25°C	I	−10	±1	+10	−10	±1	+10	%
Rise/Fall Time, 5 pF Load	25°C	V		2			2		ns
Toggle Rate, High Z Load	25°C	IV	300	350		300	350		MHz
Toggle Rate, 50 Ω Load	25°C	IV	375	400		375	400		MHz
Output Cycle-to-Cycle Jitter[8]		IV			4.0			4.0	Ps rms

Parameter	Temp	Test Level	AD9854ASQ			AD9854AST			Unit
			Min	Typ	Max	Min	Typ	Max	
COMPARATOR NARROW-BAND SFDR[9]									
10 MHz (±1 MHz)	25°C	V		84			84		dBc
10 MHz (±250 MHz)	25°C	V		84			84		dBc
10 MHz (±50 MHz)	25°C	V		92			92		dBc
41 MHz (±1 MHz)	25°C	V		76			76		dBc
41 MHz (±250 MHz)	25°C	V		82			82		dBc
41 MHz (±50 MHz)	25°C	V		89			89		dBc
119 MHz (±1 MHz)	25°C	V		73					dBc
119 MHz (±250 MHz)	25°C	V		73					dBc
119 MHz (±50 MHz)	25°C	V		83					dBc
CLOCK GENERATOR OUTPUT JITTER									
5 MHz A_{OUT}	25°C	V		23			23		Ps rms
40 MHz A_{OUT}	25°C	V		12			12		Ps rms
100 MHz A_{OUT}	25°C	V		7			7		Ps rms
PARALLEL I/O TIMING CHARACTERISTICS									
T_{ASU} (Address Setup Time to $\overline{WR}$ Signal Active)	Full	IV	8.0	7.5		8.0	7.5		ns
T_{ADHW} (Address Hold Time to $\overline{WR}$ Signal Inactive)	Full	IV	0			0			ns
T_{DSU} (Data Setup Time to $\overline{WR}$ Signal Inactive)	Full	IV	3.0	1.6		3.0	1.6		ns
T_{DHD} (Data Hold Time to $\overline{WR}$ Signal Inactive)	Full	IV		0		0			ns
T_{WRLOW} ($\overline{WR}$ Signal Minimum Low Time)	Full	IV	2.5	1.8		2.5	1.8		ns
T_{WRHIGH} ($\overline{WR}$ Signal Minimum High Time)	Full	IV	7			7			ns
T_{WR} (Minimum Write Time)	Full	IV	10.5			10.5			ns
T_{ADV} (Address to Data Valid Time)	Full	V	15		15	15		15	ns
T_{ADHR} (Address Hold Time to $\overline{RD}$ Signal Inactive)	Full	IV	5			5			ns
T_{RDLOV} ($\overline{RD}$ Low-to-Output Valid)	Full	IV			15			15	ns
T_{RDHOZ} ($\overline{RD}$ High-to-Data Three-State)	Full	IV			10			10	ns
SERIAL I/O TIMING CHARACTERISTICS									
T_{PRE} ($\overline{CS}$ Setup Time)	Full	IV	30			30			ns
T_{SCLK} (Period of Serial Data Clock)	Full	IV	100			100			ns
T_{DSU} (Serial Data Setup Time)	Full	IV	30			30			ns
$T_{SCLKPWH}$ (Serial Data Clock Pulse Width High)	Full	IV	40			40			ns
$T_{SCLKPWL}$ (Serial Data Clock Pulse Width Low)	Full	IV	40			40			ns
T_{DHLD} (Serial Data Hold Time)	Full	IV	0			0			ns
T_{DV} (Data Valid Time)	Full	V		30			30		ns
CMOS LOGIC INPUTS[10]									
Logic 1 Voltage	25°C	I	2.2			2.2			V
Logic 0 Voltage	25°C	I			0.8			0.8	V
Logic 1 Current	25°C	IV			±5			±12	µA
Logic 0 Current	25°C	IV			±5			±12	µA
Input Capacitance	25°C	V		3			3		pF
POWER SUPPLY[11]									
$+V_S$ Current[12]	25°C	I		1050	1210		755	865	mA
$+V_S$ Current[13]	25°C	I		710	816		515	585	mA
$+V_S$ Current[14]	25°C	I		600	685		435	495	mA
P_{DISS}	25°C	I		3.475	4.190		2.490	3.000	W
P_{DISS}	25°C	I		2.345	2.825		1.700	2.025	W
P_{DISS}	25°C	I		1.975	2.375		1.435	1.715	W
P_{DISS} Power-Down Mode	25°C	I		1	50		1	50	mW

[1] The reference clock inputs are configured to accept a 1 V p-p (typical) dc offset square or sine wave centered at one-half the applied V_{DD} or a 3 V TTL-level pulse input.
[2] An internal 400 mV p-p differential voltage swing equates to 200 mV p-p applied to both REFCLK input pins.
[3] The I and Q gain imbalance is digitally adjustable to less than 0.01 dB.
[4] Pipeline delays of each individual block are fixed; however, if the eight top MSBs of a tuning word are all zeros, the delay appears longer. This is due to insufficient phase accumulation per a system CLK period to produce enough LSB amplitude to the D/A converter.
[5] If a feature such as the inverse sinc, which has 16 pipeline delays, can be bypassed, the total delay is reduced by that amount.
[6] The I/O update CLK transfers data from the I/O port buffers to the programming registers. This transfer is measured in system clocks.
[7] Change in duty cycle from 1 MHz to 100 MHz with 1 V p-p sine wave input and 0.5 V threshold.
[8] Represents comparator's inherent cycle-to-cycle jitter contribution. Input signal is a 1 V, 40 MHz square wave. Measurement device Wavecrest DTS – 2075.
[9] Comparator input originates from analog output section via external 7-pole elliptic LPF. Single-ended input, 0.5 V p-p. Comparator output terminated in 50 Ω.
[10] Avoid overdriving digital inputs. (Refer to equivalent circuits in Figure 3.)
[11] Simultaneous operation at the maximum ambient temperature of 85°C and the maximum internal clock frequency of 200 MHz for the 80-lead LQFP, or 300 MHz for the thermally enhanced 80-lead LQFP, may cause the maximum die junction temperature of 150°C to be exceeded. Refer to the Power Dissipation and Thermal Considerations section for derating and thermal management information.
[12] All functions engaged.
[13] All functions except inverse sinc engaged.
[14] All functions except inverse sinc and digital multipliers engaged.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
V_S	4 V
Digital Inputs	−0.7 V to $+V_S$
Digital Output Current	5 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
Lead Temperature (Soldering, 10 s)	300°C
Maximum Clock Frequency (ASQ)	300 MHz
Maximum Clock Frequency (AST)	200 MHz
θ_{JA} (ASQ)	16°C/W
θ_{JA} (AST)	38°C/W
θ_{JC} (ASQ)	2°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

1. 100% production tested.
3. Sample tested only.
4. Parameter is guaranteed by design and characterization testing.
5. Parameter is a typical value only.
6. Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

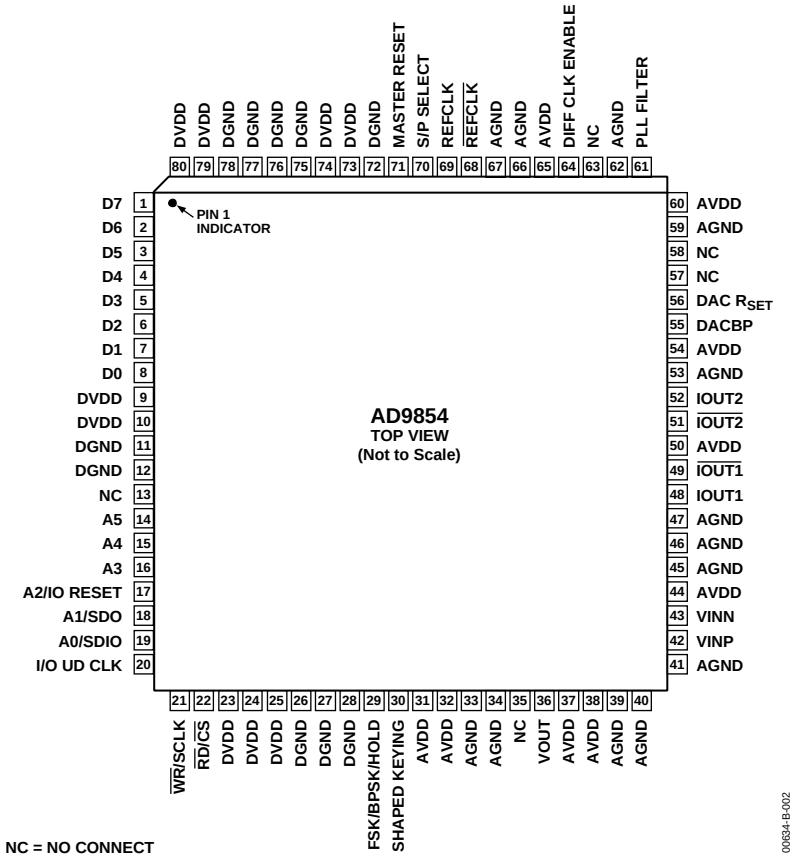

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 8	D7 to D0	8-Bit Bidirectional Parallel Programming Data Inputs. Used only in parallel programming mode.
9, 10, 23, 24, 25, 73, 74, 79, 80	DVDD	Connections for the Digital Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND.
11, 12, 26, 27, 28, 72, 75, 76, 77, 78	DGND	Connections for Digital Circuitry Ground Return. Same potential as AGND.
13, 35, 57, 58, 63	NC	No Internal Connection.
14 to 19	A5 toA0	Six-Bit Parallel Address Inputs for Program Registers. Used only in parallel programming mode. Pin 17 (A2), Pin 18 (A1), and Pin 19 (A0) have a second function when the serial programming mode is selected, as described next.
(17)	A2/IO RESET	Allows an IO RESET of the serial communications bus that is unresponsive due to improper programming protocol. Resetting the serial bus in this manner does not affect previous programming nor does it invoke the default programming values listed in Table 7. Active high.
(18)	A1/SDO	Unidirectional Serial Data Output. Used in 3-wire serial communication mode.
(19)	A0/SDIO	Bidirectional Serial Data Input/Output. Used in 2-wire serial communication mode.
20	I/O UD CLK	Bidirectional I/O Update CLK. Direction is selected in control register. If selected as an input, a rising edge transfers the contents of the I/O port buffers to the programming registers. If I/O UD CLK is selected as an output (default), an output pulse (low to high) of an eight-system-clock-cycle duration indicates that an internal frequency update has occurred.
21	$\overline{WR}$/SCLK	Write Parallel Data to I/O Port Buffers. Shared function with SCLK. Serial clock signal associated with the serial programming bus. Data is registered on the rising edge. This pin is shared with $\overline{WR}$ when the parallel mode is selected. Mode dependent on Pin 70 (S/P select).

Pin No.	Mnemonic	Description
22	$\overline{RD}/\overline{CS}$	Read Parallel Data from Programming Registers. Shared function with $\overline{CS}$. Chip-select signal associated with the serial programming bus. Active Low. This pin is shared with $\overline{RD}$ when parallel mode is selected.
29	FSK/BPSK/HOLD	Multifunction pin according to the mode of operation selected in the programming control register. In FSK mode, logic low selects F1, logic high selects F2. In BPSK mode, logic low selects Phase 1, logic high selects Phase 2. In chirp mode, logic high engages the hold function, causing the frequency accumulator to halt at its current location. To resume or commence chirp mode, logic low is asserted.
30	SHAPED KEYING	Must first be selected in the programming control register to function. A logic high causes the I and Q DAC outputs to ramp up from zero-scale to full-scale amplitude at a preprogrammed rate. Logic low causes the full-scale output to ramp down to zero scale at the preprogrammed rate.
31, 32, 37, 38, 44, 50, 54, 60, 65	AVDD	Connections for the Analog Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND.
33, 34, 39, 40, 41, 45, 46, 47, 53, 59, 62, 66, 67	AGND	Connections for Analog Circuitry Ground Return. Same potential as DGND.
36	VOUT	Internal High Speed Comparator's Noninverted Output Pin. Designed to drive 10 dBm to 50 Ω load as well as standard CMOS logic levels.
42	VINP	Voltage Input Positive. The internal high speed comparator's noninverting input.
43	VINN	Voltage Input Negative. The internal high speed comparator's inverting input.
48	IOUT1	Unipolar Current Output of the I or Cosine DAC. (Refer to Figure 3.)
49	$\overline{IOUT1}$	Complementary Unipolar Current Output of the I or Cosine DAC.
51	$\overline{IOUT2}$	Complementary Unipolar Current Output of the Q or Sine DAC.
52	IOUT2	Unipolar Current Output of the Q or Sine DAC. This DAC can be programmed to accept external 12-bit data in lieu of internal sine data, allowing the AD9854 to emulate the AD9852 control DAC function.
55	DACBP	Common Bypass Capacitor Connection for both I and Q DACs. A 0.01 µF chip capacitor from this pin to AVDD improves harmonic distortion and SFDR slightly. No connect is permissible (slight SFDR degradation).
56	DAC R_{SET}	Common Connection for both I and Q DACs to set the full-scale output current. $R_{SET} = 39.9/I_{OUT}$. Normal R_{SET} range is from 8 kΩ (5 mA) to 2 kΩ (20 mA).
61	PLL FILTER	Provides the connection for the external zero compensation network of the REFCLK multiplier's PLL loop filter. The zero compensation network consists of a 1.3 kΩ resistor in series with a 0.01 µF capacitor. The other side of the network should be connected to AVDD as close as possible to Pin 60. For optimum phase noise performance, the REFCLK multiplier can be bypassed by setting the Bypass PLL bit in Control Register 1E.
64	DIFF CLK ENABLE	Differential REFCLK Enable. A high level of this pin enables the differential clock inputs, REFCLK and $\overline{REFCLK}$ (Pins 69 and 68, respectively).
68	$\overline{REFCLK}$	The Complementary Differential Clock Signal (180 Degrees Out of Phase). User should tie this pin high or low when single-ended clock mode is selected. Same signal levels as REFCLK.
69	REFCLK	Single-Ended Reference Clock Input (CMOS Logic Levels Required) or One of Two Differential Clock Signals. In differential ref clock mode, both inputs can be CMOS logic levels or have greater than 400 mV p-p square or sine waves centered about 1.6 V dc.
70	S/P SELECT	Selects Serial Programming Mode (Logic low) or Parallel Programming Mode (Logic High).
71	MASTER RESET	Initializes the serial/parallel programming bus to prepare for user programming; sets programming registers to a do-nothing state defined by the default values listed in Table 7. Active on logic high. Asserting master reset is essential for proper operation on power-up.

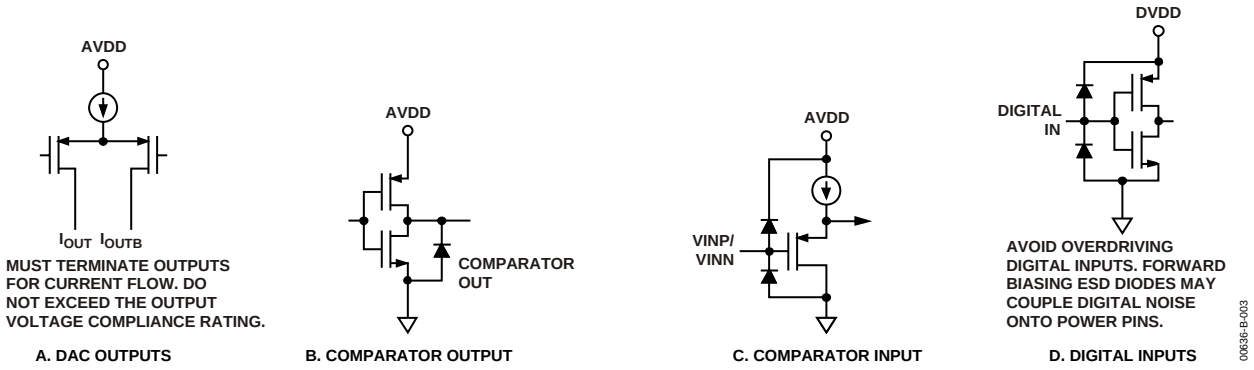

Figure 3. Equivalent Input and Output Circuits

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4 to Figure 9 indicate the wideband harmonic distortion performance of the AD9854 from 19.1 MHz to 119.1 MHz fundamental output, reference clock = 30 MHz, REFCLK multiplier = 10. Each graph plotted from 0 MHz to 150 MHz (Nyquist).

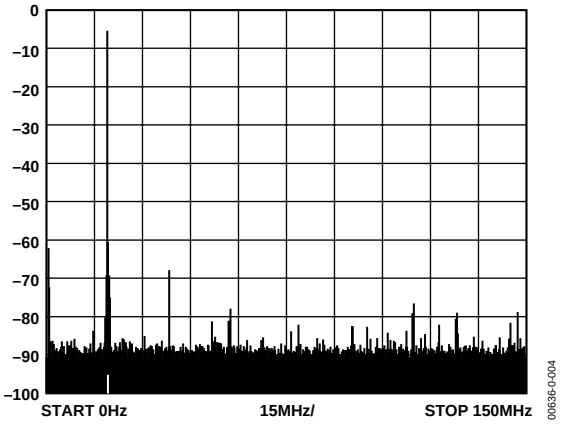

Figure 4. Wideband SFDR, 19.1 MHz

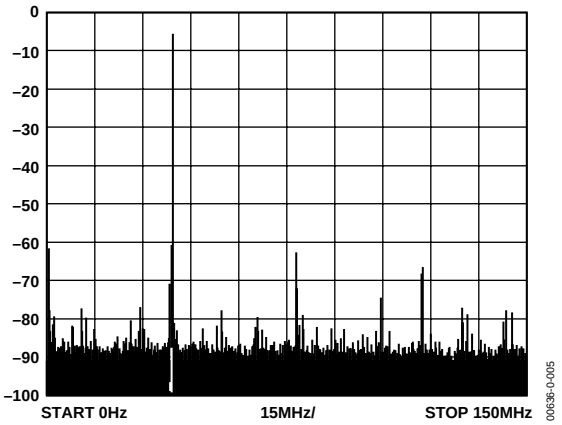

Figure 5. Wideband SFDR, 39.1 MHz

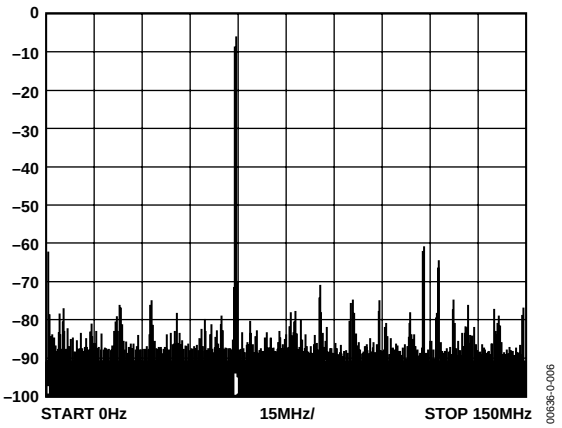

Figure 6. Wideband SFDR, 59.1 MHz

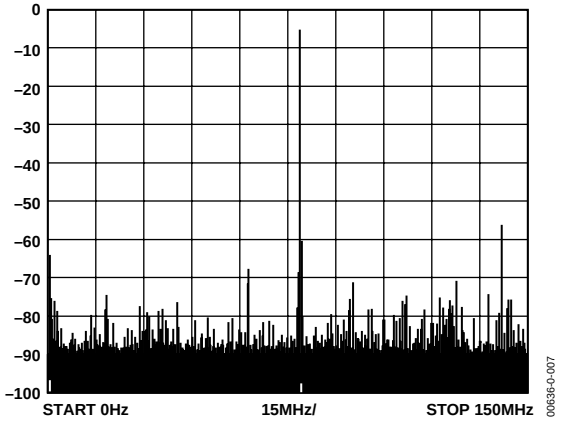

Figure 7. Wideband SFDR, 79.1 MHz

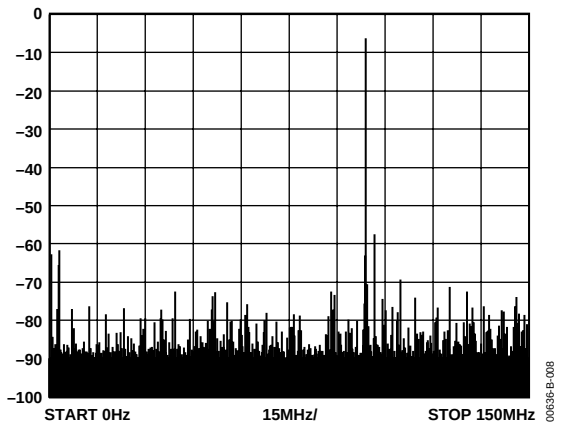

Figure 8. Wideband SFDR, 99.1 MHz

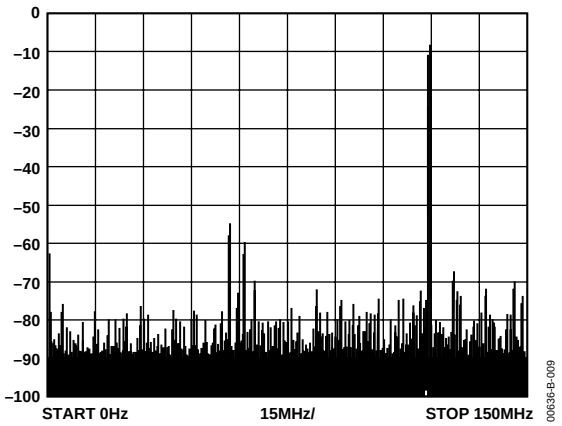

Figure 9. Wideband SFDR, 119.1 MHz

Figure 10 to Figure 13 show the trade-off in elevated noise floor, increased phase noise, and discrete spurious energy when the internal REFCLK multiplier circuit is engaged. Plots with wide (1 MHz) and narrow (50 kHz) spans are shown. Compare the noise floor of Figure 11 and Figure 13 to Figure 14 and Figure 15. The improvement seen in Figure 11 and Figure 13 is a direct result of sampling the fundamental at a higher rate. Sampling at a higher rate spreads the quantization noise of the DAC over a wider bandwidth, which effectively lowers the noise floor.

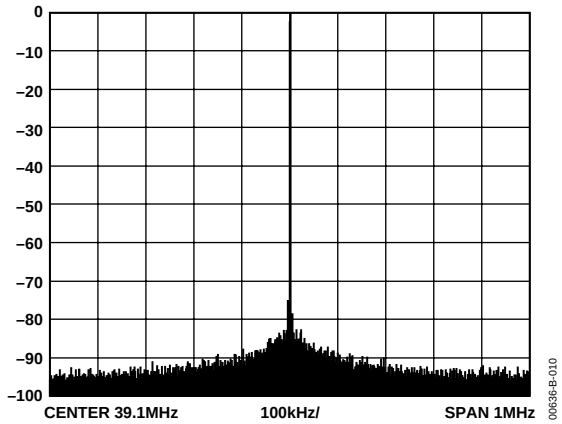

Figure 10. Narrow-Band SFDR, 39.1 MHz, 1 MHz BW, 300 MHz REFCLK with REFCLK Multiply Bypassed

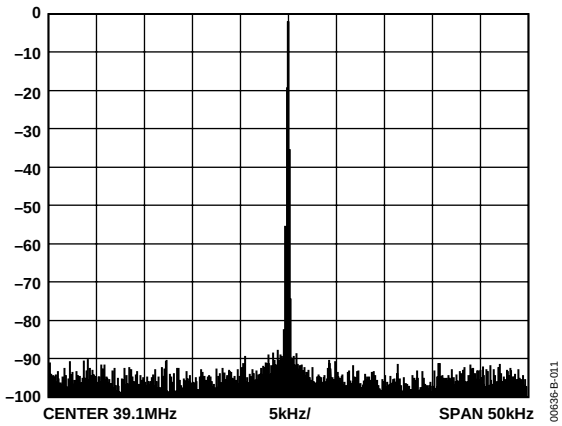

Figure 11. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 300 MHz REFCLK with REFCLK Multiply Bypassed

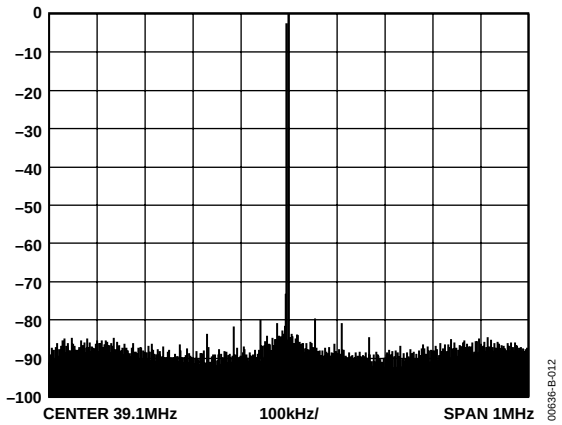

Figure 12. Narrow-Band SFDR, 39.1 MHz, 1 MHz BW, 30 MHz REFCLK with REFCLK Multiply = 10x

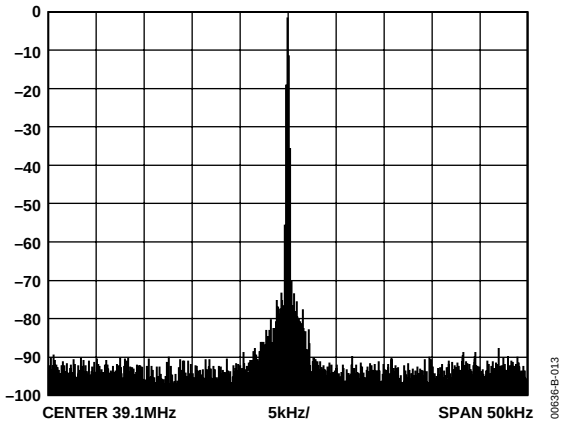

Figure 13. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 30 MHz REFCLK with REFCLK Multiply = 10x

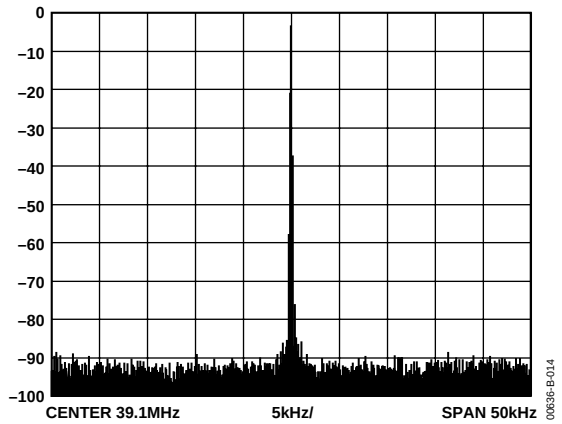

Figure 14. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 100 MHz REFCLK with REFCLK Multiply Bypassed

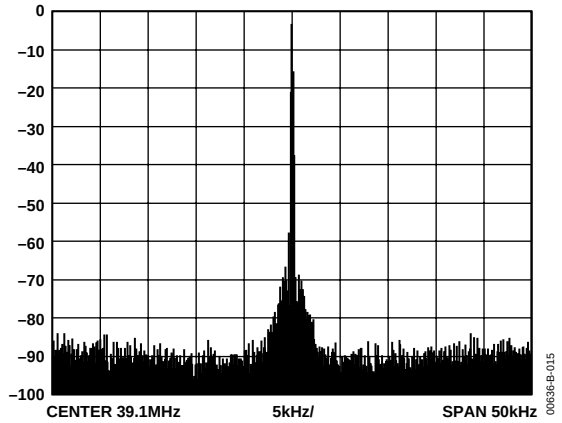

Figure 15. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 10 MHz REFCLK with REFCLK Multiply = 10x

Figure 16 and Figure 17 show the narrow-band performance of the AD9854 when operating with a 20 MHz reference clock and the REFCLK multiplier enabled at 10× vs. a 200 MHz reference clock with REFCLK multiplier bypassed.

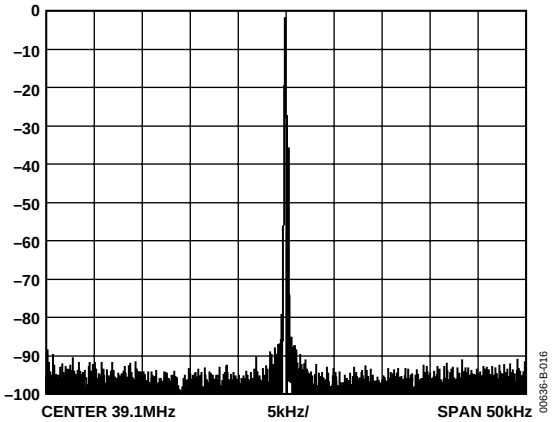

Figure 16. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 200 MHz REFCLK with REFCLK Multiply Bypassed

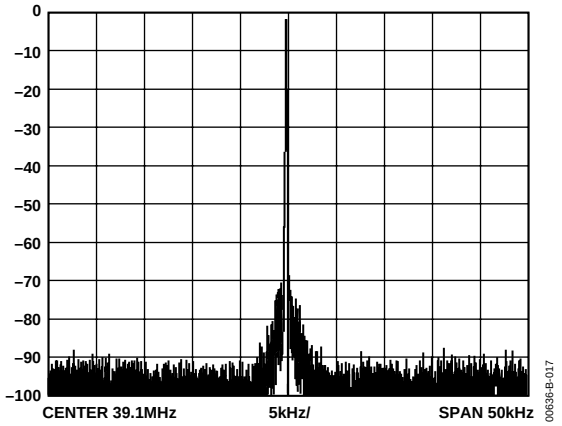

Figure 17. Narrow-Band SFDR, 39.1 MHz, 50 kHz BW, 20 MHz REFCLK with REFCLK Multiply = 10x

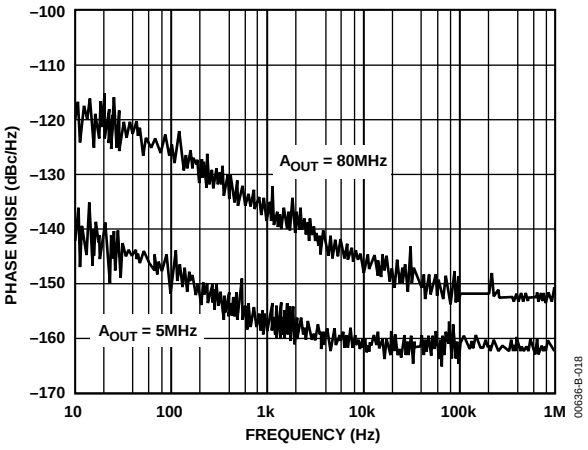

Figure 18. Residual Phase Noise, 300 MHz REFCLK with REFCLK Multiplier Bypassed

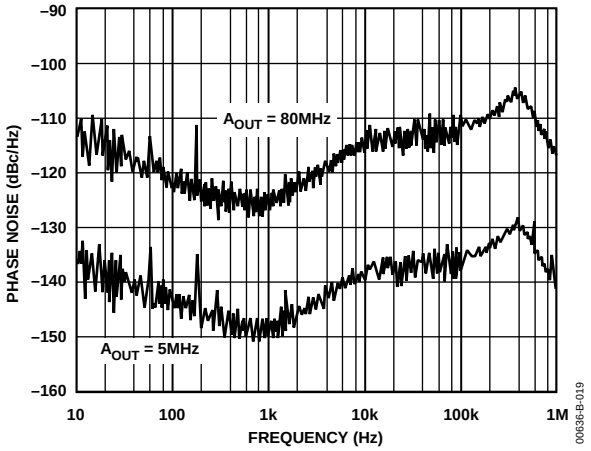

Figure 19. Residual Phase Noise, 30 MHz REFCLK with REFCLK Multiplier = 10x

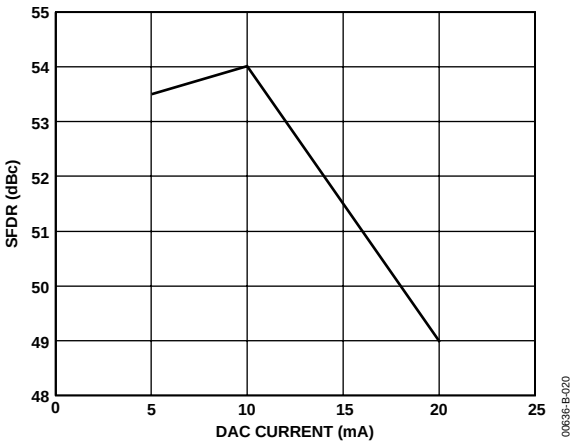

Figure 20. SFDR vs. DAC Current, 59.1 A_{OUT}, 300 MHz REFCLK with REFCLK Multiplier Bypassed

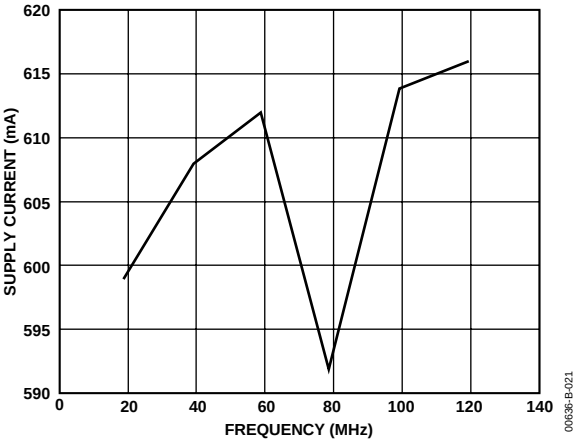

Figure 21. Supply Current vs. Output Frequency; Variation Is Minimal as a Percentage and Heavily Dependent on Tuning Word

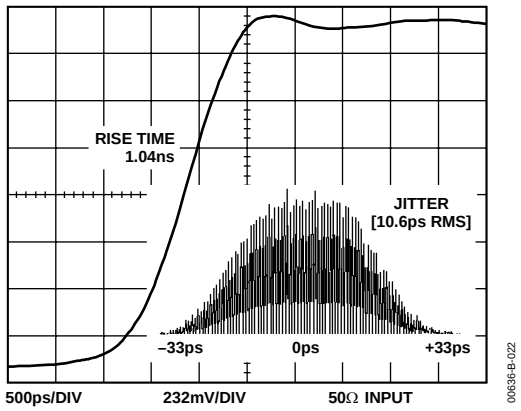

Figure 22. Typical Comparator Output Jitter, 40 MHz A_{OUT}, 300 MHz RFCLK with REFCLK Multiplier Bypassed

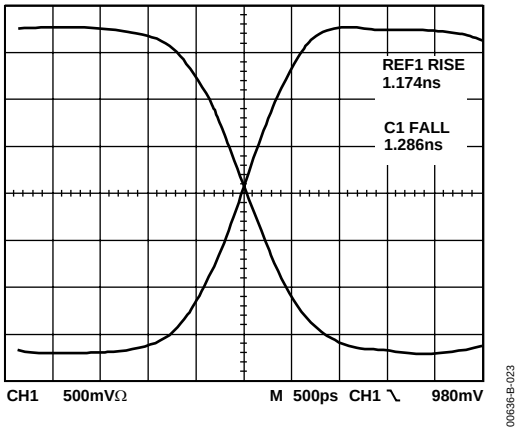

Figure 23. Comparator Rise/Fall Times

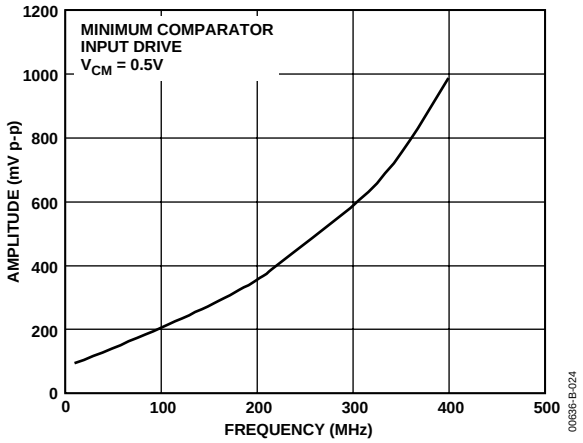

Figure 24. Comparator Toggle Voltage Requirement

TYPICAL APPLICATIONS

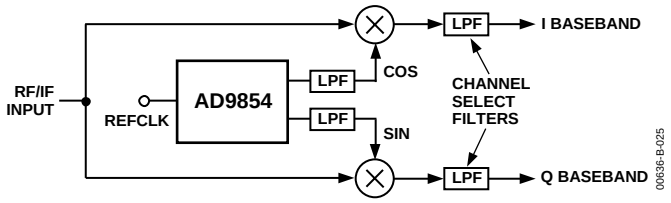

Figure 25. Quadrature Downconversion

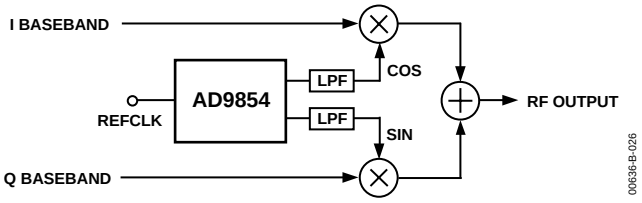

Figure 26. Direct Conversion Quadrature Upconverter

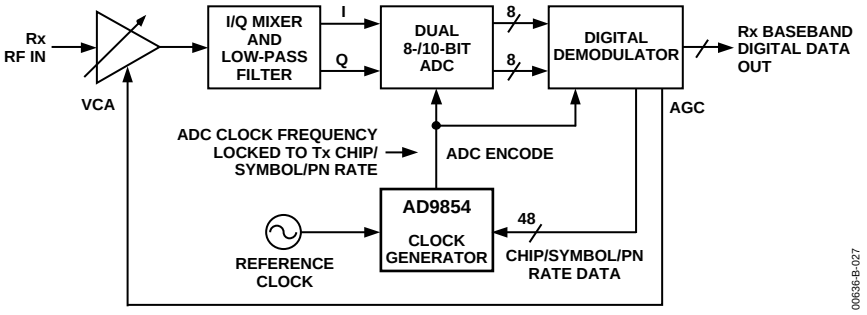

Figure 27. Chip Rate Generator in Spread Spectrum Application

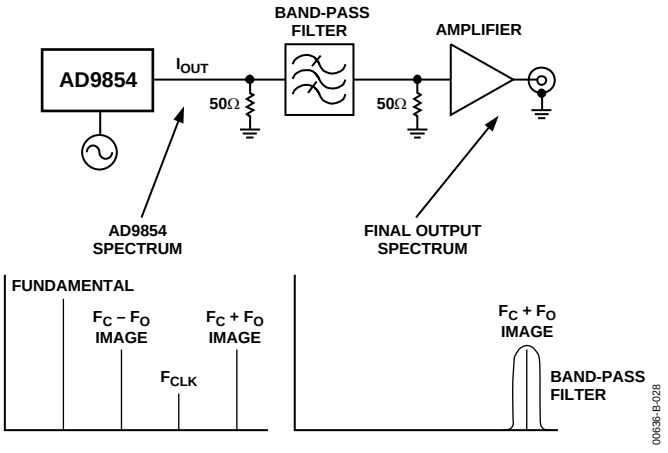

Figure 28. Using an Aliased Image to Generate a High Frequency

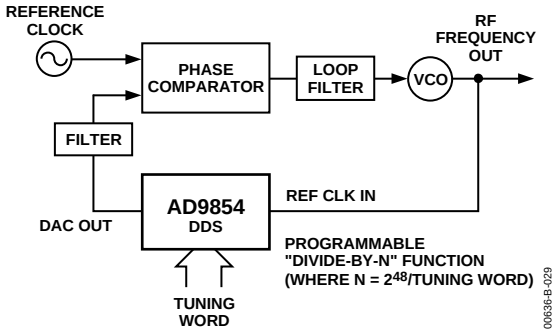

Figure 29. Programmable Fractional Divide-by-N Synthesizer

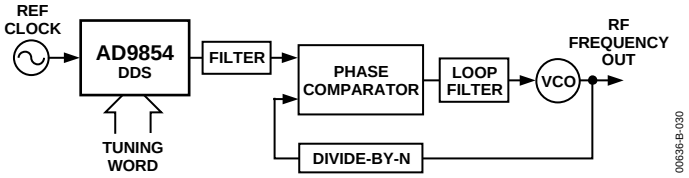

Figure 30. Agile High Frequency Synthesizer

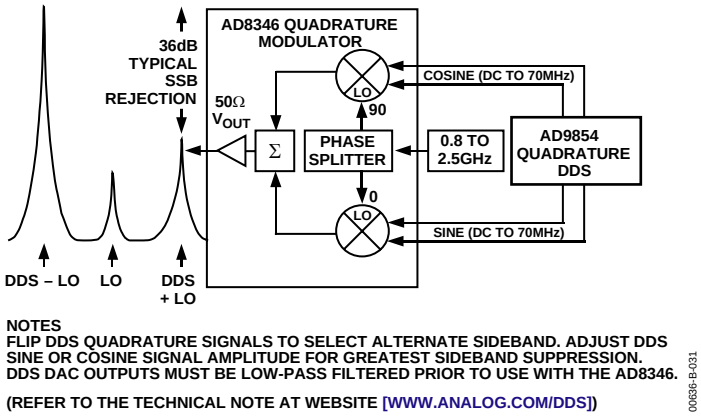

Figure 31. Single Sideband Upconversion

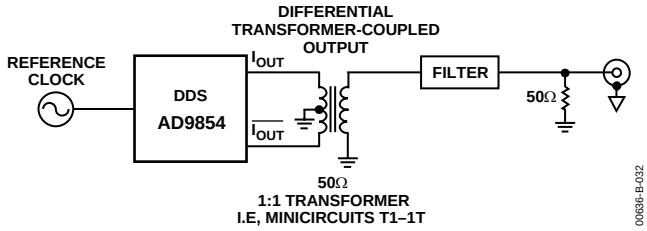

Figure 32. Differential Output Connection for Reduction of Common-Mode Signals

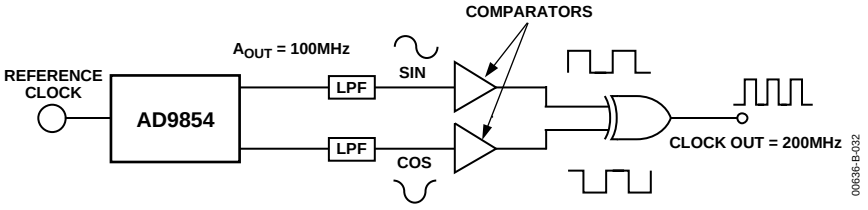

Figure 33. Clock Frequency Doubler

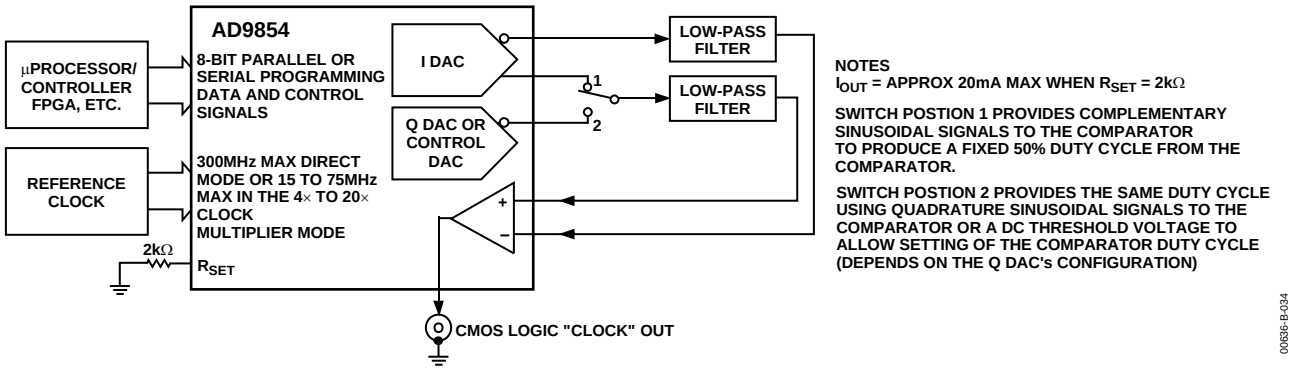

Figure 34. Frequency Agile Clock Generator Applications for the AD9854

THEORY OF OPERATION

The AD9854 quadrature output digital synthesizer is a highly flexible device that addresses a wide range of applications. The device consists of an NCO with a 48-bit phase accumulator, a programmable reference clock multiplier, inverse sinc filters, digital multipliers, two 12-bit/300 MHz DACs, a high speed analog comparator, and interface logic. This highly integrated device can be configured to serve as a synthesized LO, agile clock generator, and FSK/BPSK modulator.

Analog Devices, Inc. provides a technical tutorial about the operational theory of the functional blocks of the device. The tutorial includes a technical description of the signal flow through a DDS device and provides basic applications information for a variety of digital synthesis implementations. The document, "A Technical Tutorial on Digital Signal Synthesis," is available from the DDS Technical Library, on the Analog Devices DDS website at www.analog.com/dds.

MODES OF OPERATION

The AD9854 has five programmable operational modes. To select a mode, three bits in the control register (parallel Address 1F hex) must be programmed, as described in Table 4.

Table 4. Mode Selection Table

Mode 2	Mode 1	Mode 0	Result
0	0	0	Single Tone
0	0	1	FSK
0	1	0	Ramped FSK
0	1	1	Chirp
1	0	0	BPSK

In each mode, some functions may not be permitted. Table 5 lists the functions and their availability for each mode.

Single-Tone (Mode 000)

This is the default mode when master reset is asserted. It may also be accessed if it is user programmed into the control register. The phase accumulator, responsible for generating an output frequency, is presented with a 48-bit value from Frequency Tuning Word 1 registers whose default values are zero. Default values from the remaining applicable registers further define the single-tone output signal qualities.

The default values after a master reset configure the device with an output signal of 0 Hertz, 0 phase. At power-up and reset, the output from the I and Q DACs is a dc value equal to the midscale output current. This is the default mode amplitude setting of zero. See the Shaped On/Off Keying section for more details about the output amplitude control. All or some of the 28 program registers must be programmed to realize a user-defined output signal.

Figure 35 shows the transition from the default condition (0 Hz) to a user-defined output frequency (F1).

Table 5. Functions Availabile for Modes

	Mode				
Function	**Single-Tone**	**FSK**	**Ramped FSK**	**Chirp**	**BPSK**
Phase Adjust 1	✓	✓	✓	✓	✓
Phase Adjust 2					✓
Single-Pin FSK/BPSK or HOLD		✓	✓	✓	✓
Single-Pin Shaped-Keying	✓	✓	✓	✓	✓
Phase Offset or Modulation	✓	✓	✓	✓	
Amplitude Control or Modulation	✓	✓	✓	✓	✓
Inverse SINC Filter	✓	✓	✓	✓	✓
Frequency Tuning Word 1	✓	✓	✓	✓	✓
Frequency Tuning Word 2		✓	✓		
Automatic Frequency Sweep			✓	✓	

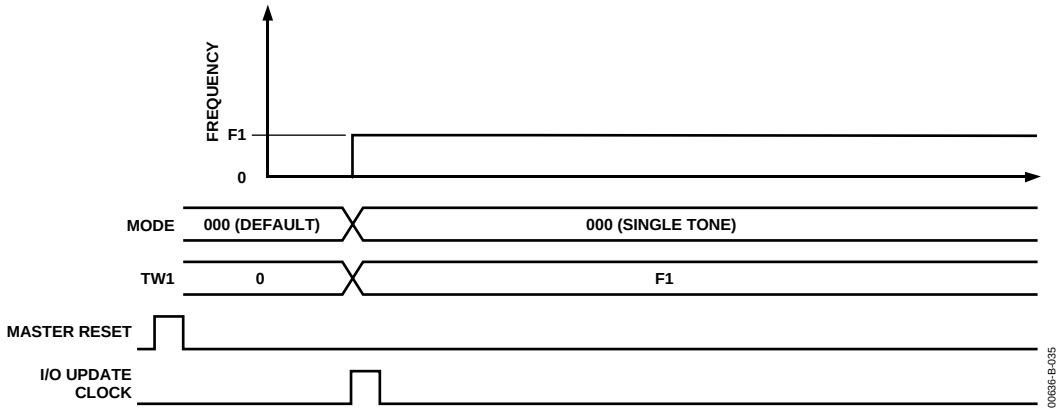

Figure 35. Default State to User-Defined Output Transition

As with all Analog Devices DDS devices, the value of the frequency tuning word is determined by

$$FTW = (Desired\ Output\ Frequency \times 2^N)/SYSCLK$$

where:
N is the phase accumulator resolution (48 bits in this instance).
Frequency is expressed in Hz.
FTW (frequency tuning word) is a decimal number.

Once a decimal number has been calculated, it must be rounded to an integer and then converted to binary format—a series of 48 binary-weighted 1s or 0s. The fundamental sine wave DAC output frequency range is from dc to 1/2 SYSCLK.

Changes in frequency are phase continuous, which means that the first sampled phase value of the new frequency is referenced in time from the last sampled phase value of the previous frequency.

The I and Q DACs of the AD9854 are always 90° out of phase. The 14-bit phase registers do not independently adjust the phase of each DAC output. Instead, both DACs are affected equally by a change in phase offset.

The single-tone mode allows the user to control the following signal qualities:

- Output frequency to 48-bit accuracy
- Output amplitude to 12-bit accuracy
  - Fixed, user-defined, amplitude control
  - Variable, programmable amplitude control
  - Automatic, programmable, single-pin-controlled, shaped on/off keying
- Output phase to 14-bit accuracy

All of these qualities can be changed or modulated via the 8-bit parallel programming port at a 100 MHz parallel-byte rate or at a 10 MHz serial rate. Incorporating this attribute permits FM, AM, PM, FSK, PSK, and ASK operation in single-tone mode.

Unramped FSK (Mode 001)

When selected, the output frequency of the DDS is a function of the values loaded into Frequency Tuning Word Register 1 and 2 and the logic level of Pin 29 (FSK/BPSK/HOLD). A logic low on Pin 29 chooses F1 (Frequency Tuning Word 1, Parallel Address 4 to 9 hex) and a logic high chooses F2 (Frequency Tuning Word 2, Parallel Register Address A to F hex). Changes in frequency are phase continuous and are internally coincident with the FSK data pin (29); however, there is deterministic pipeline delay between the FSK data signal and the DAC output. (Please refer to pipeline delays in Table 1.)

The unramped FSK mode, shown in Figure 36, represents traditional FSK, Radio Teletype (RTTY), or Teletype (TTY) transmission of digital data. FSK is a very reliable means of digital communication; however, it makes inefficient use of the bandwidth in the RF spectrum. Ramped FSK, shown in Figure 37, is a method of conserving bandwidth.

Ramped FSK (Mode 010)

This mode is a method of FSK whereby changes from F1 to F2 are not instantaneous but, instead, are accomplished in a frequency sweep or ramped fashion (the ramped notation implies that the sweep is linear). While linear sweeping or frequency ramping is easily and automatically accomplished, it is only one of many schemes. Other frequency transition schemes may be implemented by changing the ramp rate and ramp step size on-the-fly, in piecewise fashion.

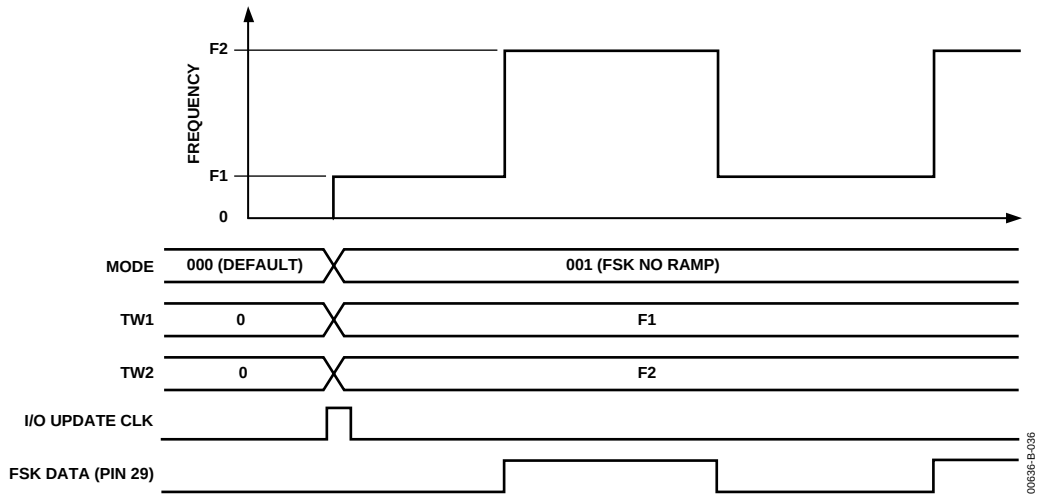

Figure 36. Traditional FSK Mode

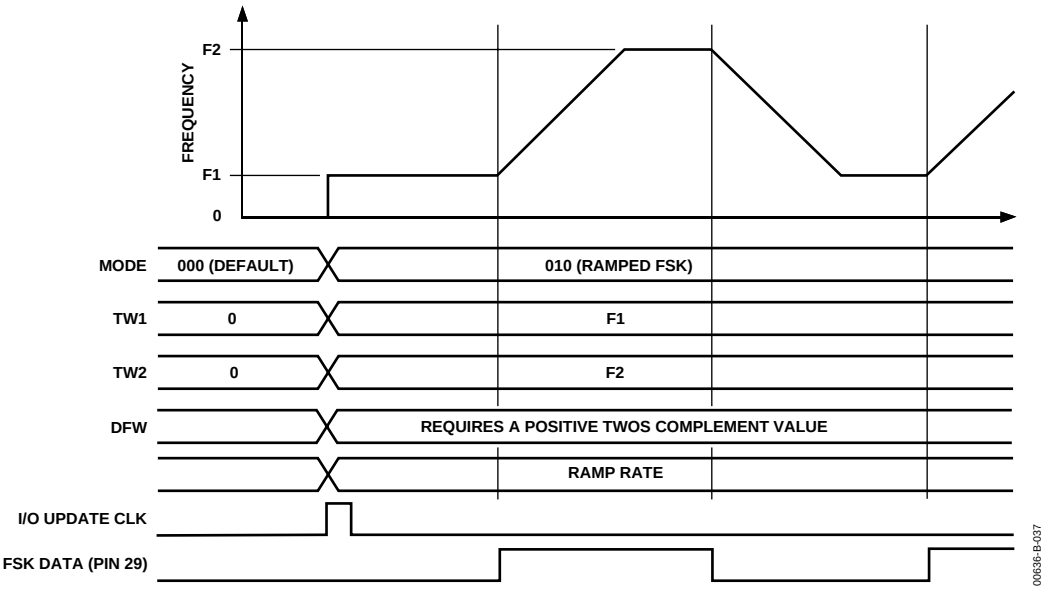

Figure 37. Ramped FSK Mode

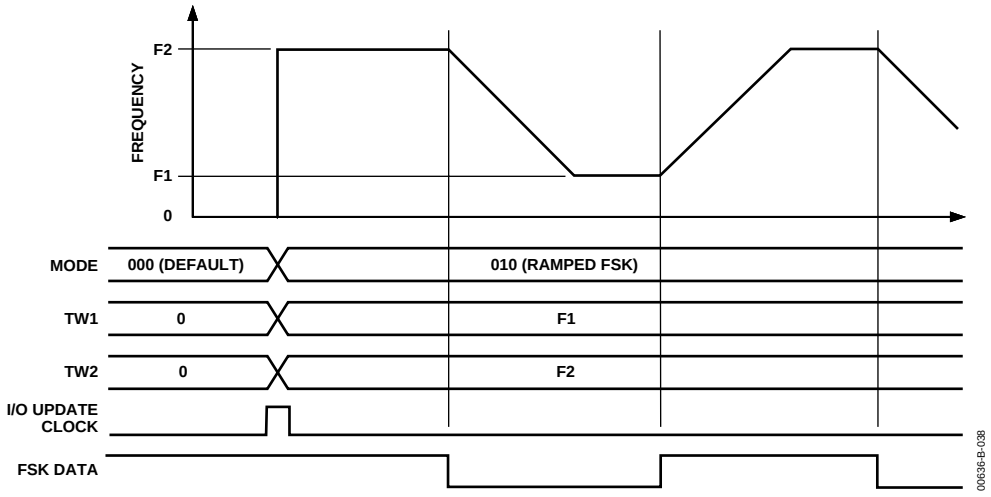

Figure 38. Ramped FSK Mode

Frequency ramping, whether linear or nonlinear, necessitates that many intermediate frequencies between F1 and F2 are output in addition to the primary F1 and F2 frequencies. Figure 37 and Figure 38 depict the frequency vs. time characteristics of a linear ramped FSK signal.

Note that in ramped FSK mode, the delta frequency (DFW) is required to be programmed as a positive twos complement value. Another requirement is that the lowest frequency (F1) be programmed in the Frequency Tuning Word 1 register.

The purpose of ramped FSK is to provide better bandwidth containment than traditional FSK by replacing the instantaneous frequency changes with more gradual, user-defined frequency changes. The dwell time at F1 and F2 can be equal to, or much greater than, the time spent at each intermediate frequency. The user controls the dwell time at F1 and F2, the number of intermediate frequencies, and the time spent at each frequency. Unlike unramped FSK, ramped FSK requires the lowest frequency to be loaded into F1 registers and the highest frequency into F2 registers.

Several registers must be programmed to instruct the DDS on the resolution of intermediate frequency steps (48 bits) and the time spent at each step (20 bits). Furthermore, the CLR ACC1 bit in the control register should be toggled (low-high-low) prior to operation to ensure that the frequency accumulator is starting from an all zeros output condition. For piecewise, nonlinear frequency transitions, it is necessary to reprogram the registers while the frequency transition is in progress to affect the desired response.

Parallel Register Addresses 1A to 1C hex comprise the 20-bit ramp rate clock registers. This is a countdown counter that outputs a single pulse whenever the count reaches zero. The counter is activated any time a logic level change occurs on FSK input Pin 29. This counter is run at the system clock rate, 300 MHz maximum. The time period between each output pulse is given as

$$(N + 1) \times (\textit{System Clock Period})$$

where N is the 20-bit ramp rate clock value programmed by the user.

The allowable range of N is from 1 to $(2^{20} - 1)$. The output of this counter clocks the 48-bit frequency accumulator shown in Figure 39. The ramp rate clock determines the amount of time spent at each intermediate frequency between F1 and F2. The counter stops automatically when the destination frequency is achieved. The dwell time spent at F1 and F2 is determined by the duration that the FSK input, Pin 29, is held high or low after the destination frequency has been reached.

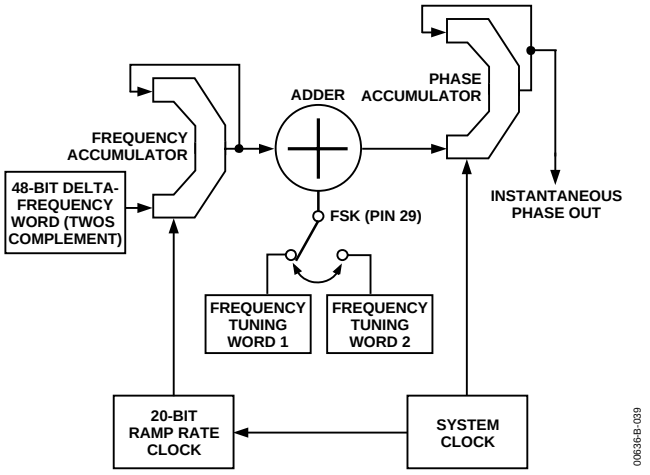

Figure 39. Block Diagram of Ramped FSK Function

Parallel Register Addresses 10 to 15 hex comprise the 48-bit, twos complement, delta frequency word registers. This 48-bit word is accumulated (added to the accumulator's output) every time it receives a clock pulse from the ramp rate counter. The output of this accumulator is then added to or subtracted from the F1 or F2 frequency word, which is then fed to the input of the 48-bit phase accumulator that forms the numerical phase steps for the sine and cosine wave outputs. In this fashion, the output frequency is ramped up and down in frequency, according to the logic state of Pin 29. The rate at which this happens is a function of the 20-bit ramp rate clock. Once the destination frequency is achieved, the ramp rate clock is stopped, which halts the frequency accumulation process.

Generally speaking, the delta frequency word is a much smaller value compared to that of the F1 or F2 tuning word. For example, if F1 and F2 are 1 kHz apart at 13 MHz, the delta frequency word might be only 25 Hz.

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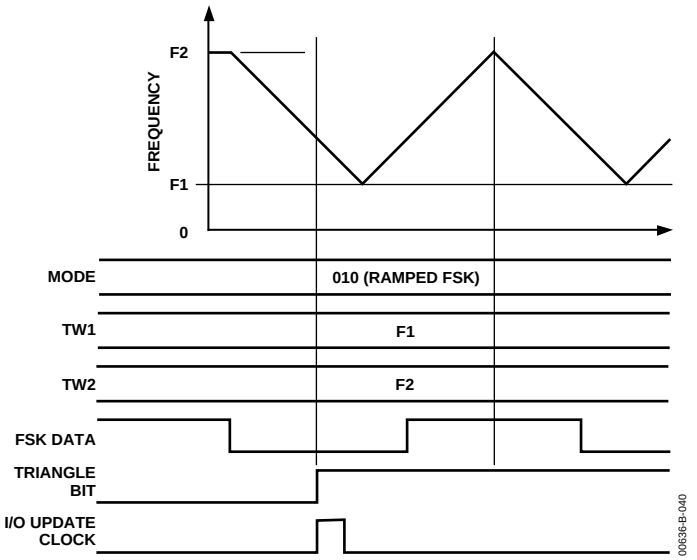


Figure 40. Effect of Triangle Bit in Amped FSK Mode

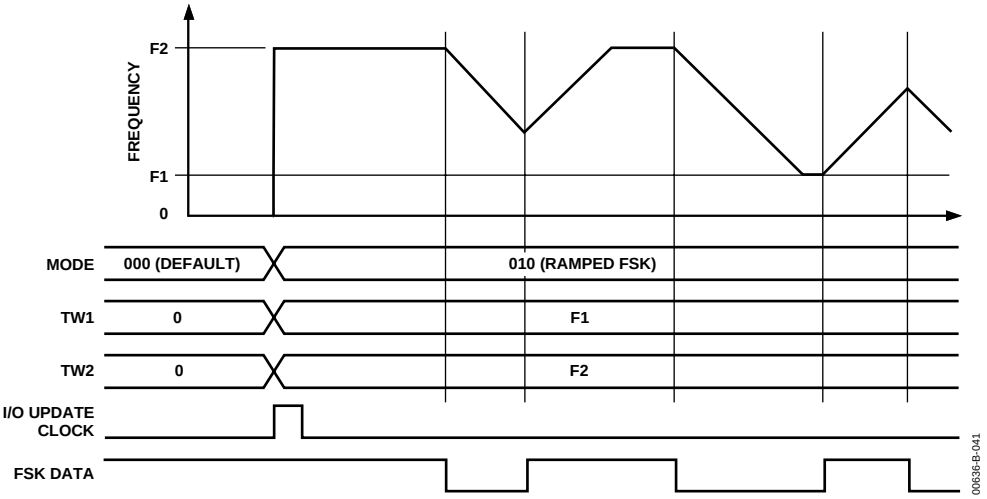


Figure 41. Effect of Premature Ramped FSK Data

Figure 41 shows that premature toggling causes the ramp to immediately reverse itself and proceed at the same rate and resolution back to the originating frequency.

The control register contains a triangle bit at Parallel Register Address 1F hex. Setting this bit high in Mode 010 causes an automatic ramp-up and ramp-down between F1 and F2 to occur without toggling Pin 29, as shown in Figure 40. The logic state of Pin 29 has no effect once the triangle bit is set high. This function uses the ramp rate clock time period and the delta frequency word step size to form a continuously sweeping linear ramp from F1 to F2 and back to F1 with equal dwell times at every frequency. Using this function, one can automatically sweep between any two frequencies from dc to Nyquist.

In the ramped FSK mode, with the triangle bit set high, an automatic frequency sweep begins at either F1 or F2, according to the logic level on Pin 29 (FSK input pin) when the triangle bit's rising edge occurs (Figure 42). If the FSK data bit is high instead of low, F2, rather than F1, is chosen as the start frequency.

Additional flexibility in the ramped FSK mode is provided in the ability to respond to changes in the 48-bit delta frequency word and/or the 20-bit ramp rate counter on the fly during the ramping from F1 to F2 or vice versa. To create these nonlinear frequency changes, it is necessary to combine several linear ramps, in a piecewise fashion, with differing slopes. This is done by programming and executing a linear ramp at some rate or slope and then altering the slope (by changing the ramp rate clock or delta frequency word or both). Changes in slope are made as often as needed to form the desired nonlinear frequency sweep response before the destination frequency is reached. These piecewise changes can be precisely timed using the 32-bit internal update clock (see the Internal and External Update Clock section).

Nonlinear ramped FSK has the appearance of a chirp function, as Figure 46 shows. The difference between a ramped FSK function and a chirp function is that FSK is limited to operation between F1 and F2. Chirp operation has no F2 limit frequency.

Two additional control bits are available in the ramped FSK mode that allow more options. CLR ACC1, Register Address 1F hex, if set high, clears the 48-bit frequency accumulator (ACC1) output with a retriggerable one-shot pulse of one system clock duration. If the CLR ACC1 bit is left high, a one-shot pulse is delivered on the rising edge of every update clock. The effect is to interrupt the current ramp, reset the frequency back to the start point, F1 or F2, and then continue to ramp up (or down) at the previous rate. This occurs even when a static F1 or F2 destination frequency is achieved.

Next, CLR ACC2 Control Bit (Register Address 1F hex) is available to clear both the frequency accumulator (ACC1) and the phase accumulator (ACC2). When this bit is set high, the output of the phase accumulator results in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators are cleared, resulting in 0 Hz output. To return to previous DDS operation, CLR ACC2 must be set to logic low.

Chirp (Mode 011)

This mode is also known as pulsed FM. Most chirp systems use a linear FM sweep pattern, but the AD9854 supports nonlinear patterns, as well. In radar applications, use of chirp or pulsed FM allows operators to significantly reduce the output power needed to achieve the same result as a single-frequency radar system would produce. Figure 43 shows a very low resolution nonlinear chirp to demonstrate the different slopes that are created by varying the time steps (ramp rate) and frequency steps (delta frequency word).

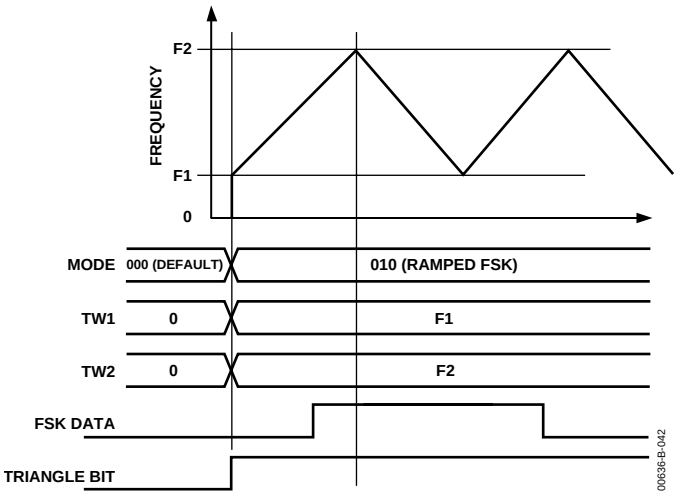


Figure 42. Automatic Linear Ramping Using the Triangle Bit

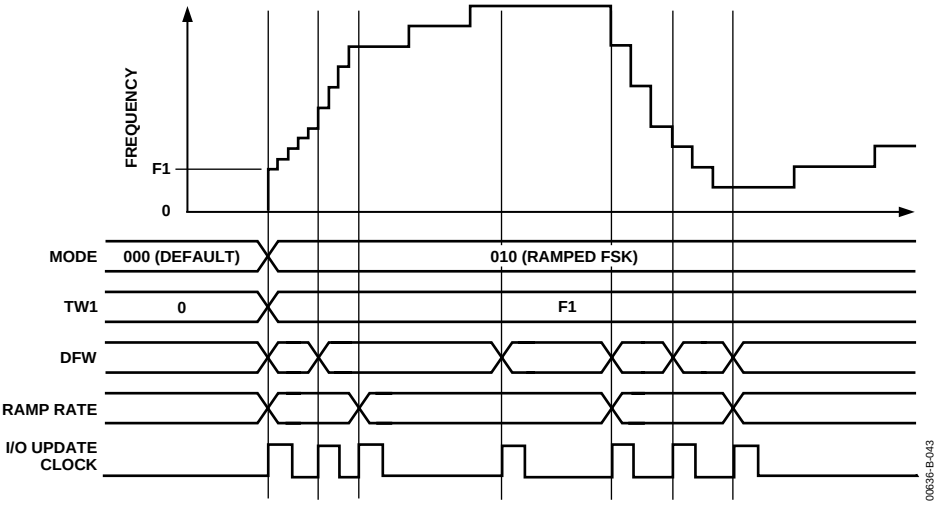


Figure 43. Example of a Nonlinear Chirp

The AD9854 permits precise, internally generated linear, or externally programmed nonlinear, pulsed or continuous FM over the complete frequency range, duration, frequency resolution, and sweep direction(s). These are all user programmable. Figure 44 shows a block diagram of the FM chirp components.

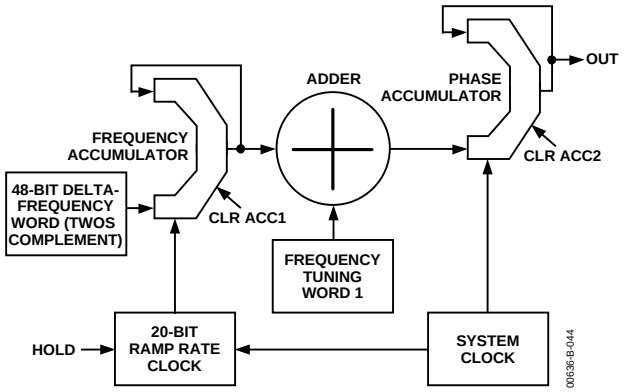


Figure 44. FM Chirp Components

Basic FM Chirp Programming Steps

1. Program a start frequency into Frequency Tuning Word 1 (FTW1) at Parallel Register Addresses 4 to 9 hex.
2. Program the frequency step resolution into the 48-bit, twos complement, delta frequency word (Parallel Register Addresses 10 to 15 hex).
3. Program the rate of change (time at each frequency) into the 20-bit ramp rate clock (Parallel Register Addresses 1A to 1C hex).

When programming is complete, an I/O update pulse at Pin 20 engages the program commands.

The necessity for a twos complement delta frequency word is to define the direction in which the FM chirp moves. If the 48-bit delta frequency word is negative (MSB is high), then the incremental frequency changes are in a negative direction from FTW1. If the 48-bit word is positive (MSB is low), then the incremental frequency changes are in a positive direction.

It is important to note that FTW1 is only a starting point for FM chirp. There is no built-in restraint requiring a return to FTW1. Once the FM chirp has begun, it is free to move, under program control, within the Nyquist bandwidth (dc to 1/2 system clock). Instant return to FTW1 is easily achieved, though, as explained next.

Two control bits are available in the FM chirp mode that allow the return to the beginning frequency, FTW1, or to 0 Hz. First, when the CLR ACC1 Bit (Register Address 1F hex) is set high, the 48-bit frequency accumulator (ACC1) output is cleared with a retriggerable one-shot pulse of one system clock duration. The 48-bit delta frequency word input to the accumulator is unaffected by CLR ACC1 bit. If the CLR ACC1 bit is held high, a one-shot pulse is delivered to the frequency accumulator (ACC1) on every rising edge of the I/O update clock. The effect is to interrupt the current chirp, reset the frequency back to FTW1, and continue the chirp at the previously programmed rate and direction. Clearing the output of the frequency accumulator in the chirp mode is illustrated in Figure 45. Shown in the diagram is the I/O update clock, which is either user supplied or internally generated.

Next, CLR ACC2 Control Bit (Register Address 1F hex) is available to clear both the frequency accumulator (ACC1) and the phase accumulator (ACC2). When this bit is set high, the output of the phase accumulator results in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators are cleared, resulting in 0 Hz output. To return to previous DDS operation, CLR ACC2 must be set to logic low. This bit is useful in generating pulsed FM.

Figure 46 illustrates the effect of the CLR ACC2 bit upon the DDS output frequency. Note that reprogramming the registers while the CLR ACC2 bit is high allows a new FTW1 frequency and slope to be loaded.

Another function that is available only in chirp mode is the hold function (Pin 29). This function stops the clock signal to the ramp rate counter, halting any further clocking pulses to the frequency accumulator, ACC1. The effect is to halt the chirp at the frequency existing just before hold was pulled high. When the Pin 29 is returned low, the clock resumes and chirp continues. During a hold condition, the user may change the programming registers; however, the ramp rate counter must resume operation at its previous rate until a count of zero is obtained before a new ramp rate count can be loaded. Figure 47 shows the hold function's effect on the DDS output frequency.

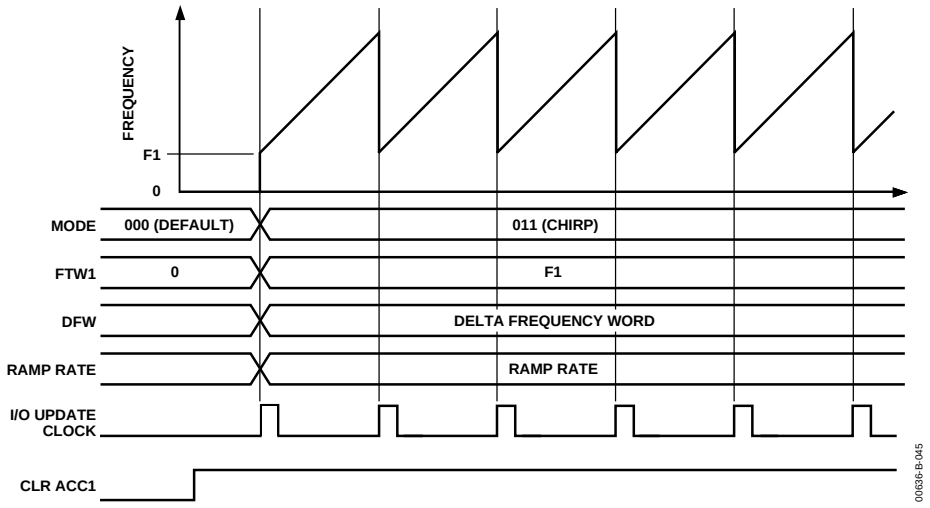


Figure 45. Effect of CLR ACC1 in FM Chirp Mode

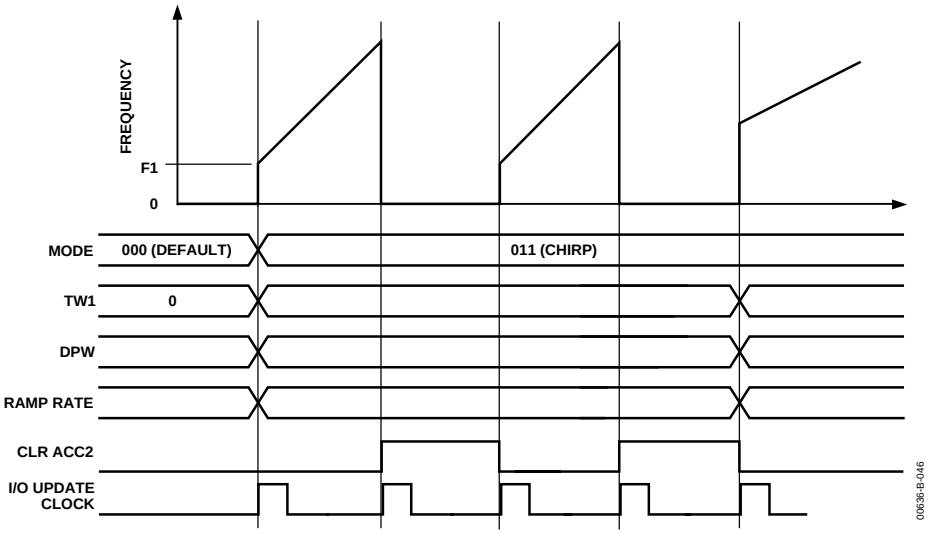


Figure 46. Effect of CLR ACC2 in Chirp Mode

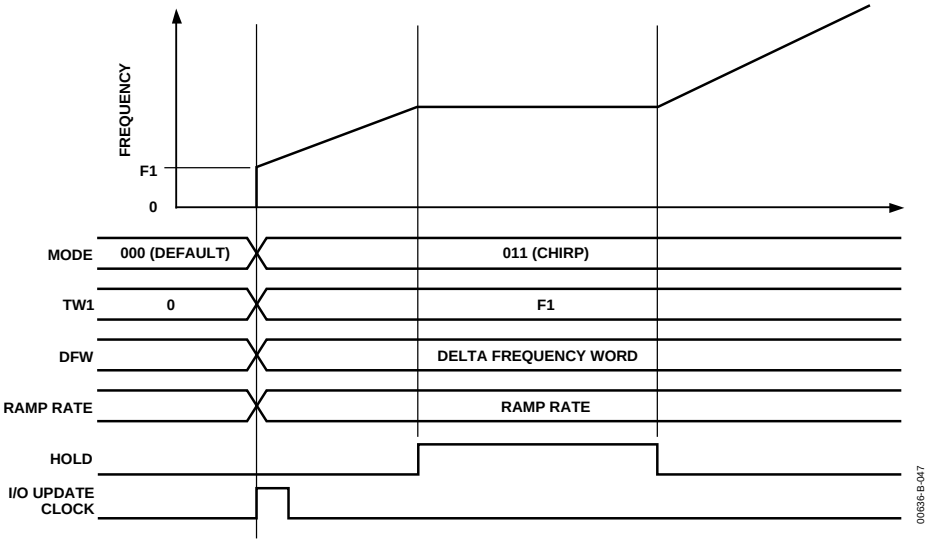


Figure 47. Illustration of Hold Function

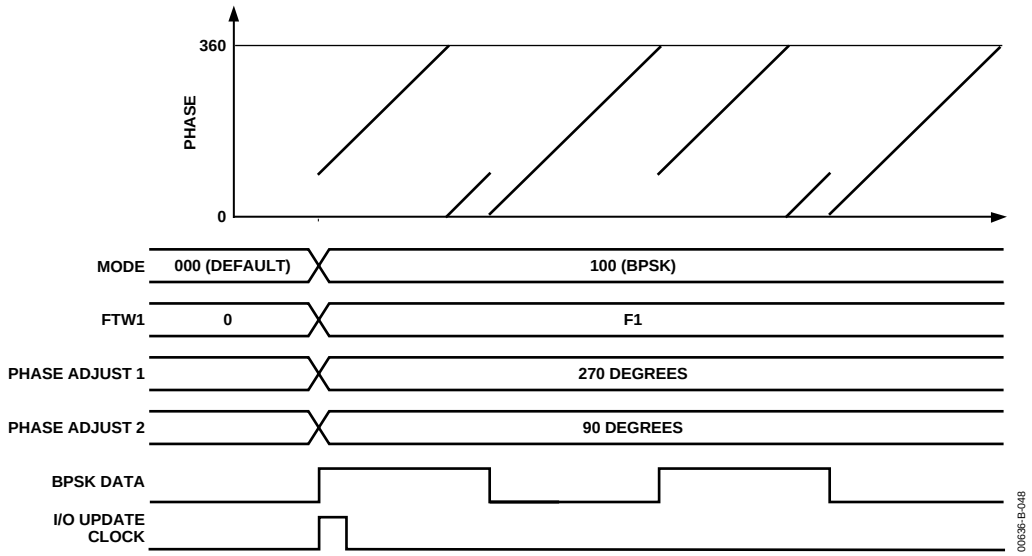


Figure 48. BPSK Mode

The 32-bit automatic I/O update counter may be used to construct complex chirp or ramped FSK sequences. Because this internal counter is synchronized with the AD9854 system clock, it allows precisely timed program changes to be invoked. In this manner, the user is only required to reprogram the desired registers before the automatic I/O update clock is generated.

In chirp mode, the destination frequency is not directly specified. If the user fails to control the chirp, the DDS naturally confines itself to the frequency range between dc and Nyquist. Unless terminated by the user, the chirp continues until power is removed.

When the chirp destination frequency is reached, the following can be done:

- Stop at the destination frequency using the hold pin, or by loading all zeros into the delta frequency word registers of the frequency accumulator (ACC1).
- Use the hold function to stop the chirp, then ramp down the output amplitude using the digital multiplier stages and the shaped keying pin, Pin 30, or via the program register control (Addresses 21 to 24 hex).
- Abruptly end the transmission with the CLR ACC2 bit.
- Continue chirp by reversing direction and returning to the previous, or another, destination frequency in a linear or user-directed manner. If this involves going down in frequency, a negative 48-bit delta frequency word (the MSB is set to 1) must be loaded into Registers 10 hex to 15 hex. Any decreasing frequency step of the delta frequency word requires the MSB to be set to logic high.
- Continue chirp by immediately returning to the beginning frequency (F1) in a saw-toothed fashion and repeat the previous chirp process. This is where the CLR ACC1 control bit is used. An automatic, repeating chirp can be set up using the 32-bit update clock to issue the CLR ACC1 command at precise time intervals. Adjusting the timing intervals or changing the delta frequency word changes the chirp range. It is incumbent upon the user to balance the chirp duration and frequency resolution to achieve the proper frequency range.

BPSK (Mode 100)

Binary, biphase, or bipolar-phase shift keying is a means to rapidly select between two preprogrammed 14-bit output phase offsets that identically affect both the I and Q outputs of the AD9854. The logic state of Pin 29, the BPSK pin, controls the selection of Phase Adjust Register 1 or 2. When low, Pin 29 selects Phase Adjust Register 1; when high, Phase Adjust Register 2 is selected. Table 7 illustrates phase changes made to four cycles of an output carrier.

Basic BPSK Programming Steps

1. Program a carrier frequency into Frequency Tuning Word 1.
2. Program the appropriate 14-bit phase words in Phase Adjust Registers 1 and 2.
3. Attach the BPSK data source to Pin 29.
4. Activate the I/O update clock when ready.

Note that for higher-order PSK modulation, the user can select the single-tone mode and program Phase Adjust Register 1 using the serial or high speed parallel programming bus.

USING THE AD9854

INTERNAL AND EXTERNAL UPDATE CLOCK

This update clock function is comprised of a bidirectional I/O pin, Pin 20, and a programmable 32-bit down counter. For programming changes to be transferred from the I/O buffer registers to the active core of the DDS, a clock signal (low-to-high edge) must be externally supplied to Pin 20 or internally generated by the 32-bit update clock.

When the user provides an external update clock, it is internally synchronized with the system clock to prevent partial transfer of program register information due to violation of data set up or hold times. This mode gives the user complete control of when updated program information becomes effective. The default mode for the update clock is internal (Int Update Clk control register bit is logic high). To switch to external update clock mode, the Int Update Clk register bit must be set to logic low. The internal update mode generates automatic, periodic update pulses with the time period set by the user.

An internally generated update clock can be established by programming the 32-bit update clock registers (Address 16 to 19 hex) and setting the Int Update Clk (Address 1F hex) control register bit to logic high. The update clock down-counter function operates at 1/2 the rate of the system clock (150 MHz maximum) and counts down from a 32-bit binary value (programmed by the user). When the count reaches 0, an automatic I/O update of the DDS output or functions is generated. The update clock is internally and externally routed on Pin 20 to allow users to synchronize programming of update information with the update clock rate. The time period between update pulses is given as

$$(N + 1) \times (System\ Clock\ Period \times 2)$$

where N is the 32-bit value programmed by the user.

The allowable range of N is from 1 to $(2^{32} - 1)$. The internally generated update pulse output on Pin 20 has a fixed high time of eight system clock cycles.

Programming the update clock register for values less than five causes the I/O UD CLK pin to remain high. The update clock functionality still works; however, the user cannot use the signal as an indication that data is transferring. This is an effect of the minimum high pulse time when I/O UD CLK is an output.

SHAPED ON/OFF KEYING

This feature allows the user to control the amplitude vs. time slope of the I and Q DAC output signals. This function is used in burst transmissions of digital data to reduce the adverse spectral impact of short, abrupt bursts of data. Users must first enable the digital multipliers by setting the OSK EN bit (Control Register Address 20 hex) to logic high in the control register. Otherwise, if the OSK EN bit is set low, the digital multipliers responsible for amplitude control are bypassed and the I and Q DAC outputs are set to full-scale amplitude. In addition to setting the OSK EN bit, a second control bit, OSK INT (also at Address 20 hex), must be set to logic high. Logic high selects the linear internal control of the output ramp-up or ramp-down function. A logic low in the OSK INT bit switches control of the digital multipliers to user-programmable 12-bit registers allowing users to dynamically shape the amplitude transition in practically any fashion. These 12-bit registers, labeled Output Shape Key I and Output Shape Key Q, are located at Addresses 21 through 24 hex, as listed in Table 7. The maximum output amplitude is a function of the R_{SET} resistor and is not programmable when OSK INT is enabled.

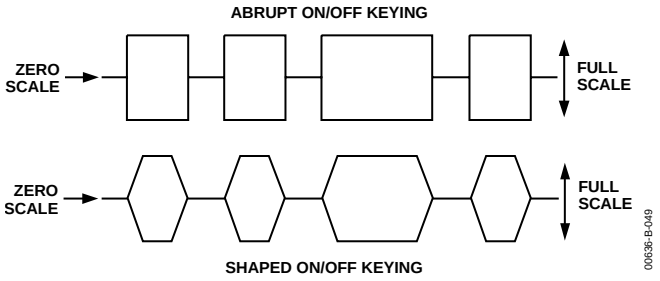


Figure 49. Shaped On/Off Keying

The transition time from zero scale to full scale must also be programmed. The transition time is a function of two fixed elements and one variable. The variable element is the programmable 8-bit ramp rate counter. This is a down counter that is clocked at the system clock rate (300 MHz max) and that generates one pulse whenever the counter reaches zero. This pulse is routed to a 12-bit counter that increments with each pulse received. The outputs of the 12-bit counter are connected to the 12-bit digital multiplier. When the digital multiplier has a value of all zeros at its inputs, the input signal is multiplied by zero, producing zero scale. When the multiplier has a value of all ones, the input signal is multiplied by a value of 4095/4096, producing nearly full scale. There are 4,094 remaining fractional multiplier values that produce output amplitudes scaled according to their binary values.

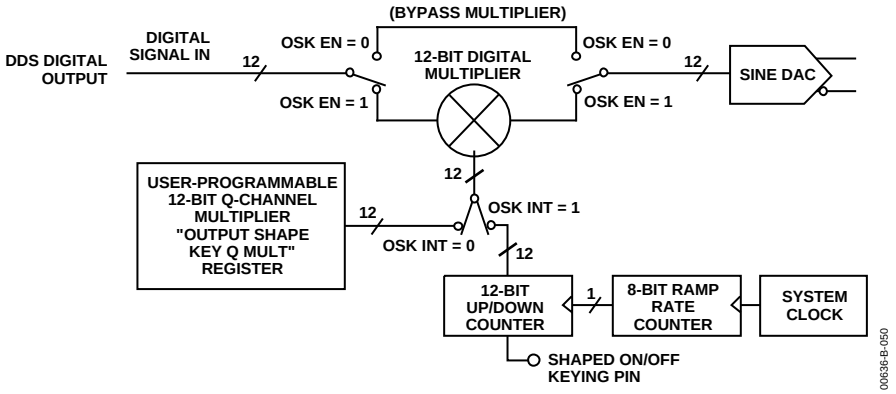


Figure 50. Block Diagram of Q-Pathway of the Digital Multiplier Section Responsible for Shaped-Keying Function

The two fixed elements of the transition time are the period of the system clock (which drives the ramp rate counter) and the number of amplitude steps (4096). To give an example, assume that the system clock of the AD9854 is 100 MHz (10 ns period). If the ramp rate counter is programmed for a minimum count of three, it takes two system clock periods (one rising edge loads the count-down value, the next edge decrements the counter from three to two). If the count-down value is less than three, the ramp rate counter stalls and, therefore, produces a constant scaling value to the digital multipliers. This stall condition may have application by the user.

The relationship of the 8-bit count-down value to the time period between output pulses is given as

$$(N + 1) \times \textit{System Clock Period}$$

where N is the 8-bit count-down value.

It takes 4096 of these pulses to advance the 12-bit up-counter from zero scale to full scale. Therefore, the minimum shaped keying ramp time for a 100 MHz system clock is

$4096 \times 4 \times 10$ ns = approximately 164 µs.

The maximum ramp time is $4096 \times 256 \times 10$ ns ≈ 10.5 ms. Finally, changing the logic state of Pin 30, shaped keying, automatically performs the programmed output envelope functions when OSK INT is high. A logic high on Pin 30 causes the outputs to linearly ramp up to full-scale amplitude and to hold until the logic level is changed to low, causing the outputs to ramp down to zero scale.

I AND Q DACS

The sine and cosine outputs of the DDS drive the Q and I DACs, respectively (300 MSPS maximum). Their maximum output amplitudes are set by the DAC R_{SET} resistor at Pin 56. These are current-out DACs with a full-scale maximum output of 20 mA; however, a nominal 10 mA output current provides best spurious-free dynamic range (SFDR) performance. The value of $R_{SET} = 39.93/I_{OUT}$, where I_{OUT} is in amps. DAC output compliance specifications limit the maximum voltage developed at the outputs to −0.5 V to +1 V. Voltages developed beyond this limitation cause excessive DAC distortion and possibly permanent damage. The user must choose a proper load impedance to limit the output voltage swing to the compliance limits. Both DAC outputs should be terminated equally for best SFDR, especially at higher output frequencies where harmonic distortion errors are more prominent.

Both DACs are preceded by inverse SIN(x)/x filters (also called inverse sinc filters) that precompensate for DAC output amplitude variations over frequency to achieve flat amplitude response from dc to Nyquist. Both DACs can be powered down by setting the DAC PD bit high (Address 1D of the control register) when not needed. I DAC outputs are designated as IOUT1 and $\overline{\text{IOUT1}}$, Pins 48 and 49, respectively. Q DAC outputs are designated as IOUT2 and $\overline{\text{IOUT2}}$, Pins 52 and 51, respectively.

CONTROL DAC

The 12-bit Q DAC can be reconfigured to perform as a control or auxiliary DAC. The control DAC output can provide dc control levels to external circuitry, generate ac signals, or enable duty cycle control of the on-board comparator. When the SRC Q DAC bit in the control register (Parallel Address 1F hex) is set high, the Q DAC inputs are switched from internal 12-bit Q data source (default setting) to external 12-bit, twos complement data, supplied by the user. Data is channeled through the serial or parallel interface to the 12-bit Q DAC register (Address 26 and 27 hex) at a maximum 100 MHz data rate. This DAC is clocked at the system clock, 300 MSPS (maximum), and has the same maximum output current capability as that of the I DAC. The single R_{SET} resistor on the AD9854 sets the full-scale output current for both DACs. The control DAC can be separately powered down for power conservation when not needed by setting the Q DAC power-down bit high (Address 1D hex). Control DAC outputs are designated as IOUT2 and $\overline{\text{IOUT2}}$ (Pins 52 and 51, respectively).

INVERSE SINC FUNCTION

The inverse sinc function precompensates input data to both DACs for the SIN(x)/x roll-off characteristic inherent in the DAC's output spectrum. This allows wide bandwidth signals (such as QPSK) to be output from the DACs without appreciable amplitude variations as a function of frequency. The inverse SINC function may be bypassed to significantly reduce power consumption, especially at higher clock speeds. When the Q DAC is configured as a control DAC, the inverse SINC function does not apply to the Q path.

Inverse SINC is engaged by default and is bypassed by bringing the Bypass Inv SINC bit high in Control Register 20 (hex), as shown in Table 7.

REFCLK MULTIPLIER

The REFCLK multiplier is a programmable PLL-based reference clock multiplier that allows the user to select an integer clock multiplying value over the range of 4× to 20×. With this function, users can input as little as 15 MHz at the REFCLK input to produce a 300 MHz internal system clock. Five bits in Control Register 1E hex set the multiplier value, as detailed in Table 6.

The REFCLK multiplier function can be bypassed to allow direct clocking of the AD9854 from an external clock source. The system clock for the AD9854 is either the output of the REFCLK multiplier (if it is engaged) or the REFCLK inputs. REFCLK may be either a single-ended or differential input by setting Pin 64, DIFF CLK ENABLE, low or high, respectively.

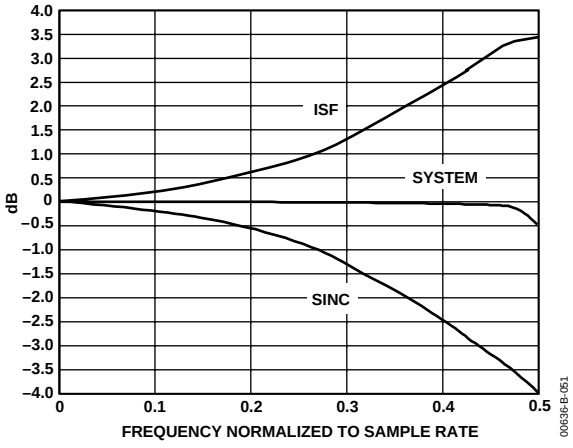


Figure 51. Inverse SINC Filter Response

PLL Range Bit

The PLL range bit selects the frequency range of the REFCLK multiplier PLL. For operation from 200 MHz to 300 MHz (internal system clock rate), the PLL range bit should be set to Logic 1. For operation below 200 MHz, the PLL range bit should be set to Logic 0. The PLL range bit adjusts the PLL loop parameters for best phase noise performance within each range.

Pin 61, PLL FILTER

This pin provides the connection for the external zero compensation network of the PLL loop filter. The zero compensation network consists of a 1.3 kΩ resistor in series with a 0.01 µF capacitor. The other side of the network should be connected as close as possible to Pin 60, AVDD. For optimum phase noise performance, the clock multiplier can be bypassed by setting the bypass PLL bit in Control Register Address 1E.

Differential REFCLK Enable

A high level on this pin enables the differential clock inputs, REFCLK and $\overline{\text{REFCLK}}$ (Pins 69 and 68, respectively). The minimum differential signal amplitude required is 400 mV p-p, at the REFCLK input pins. The center point or common-mode range of the differential signal can range from 1.6 V to 1.9 V.

When Pin 64 (DIFF CLK ENABLE) is tied low, REFCLK (Pin 69) is the only active clock input. This is referred to as single-ended mode. In this mode, Pin 68 ($\overline{\text{REFCLK}}$) should be tied low or high.

High Speed Comparator—This comparator is optimized for high speed, a >300 MHz toggle rate, low jitter, sensitive input, built-in hysteresis, and an output level of 1 V p-p minimum into 50 Ω or CMOS logic levels into high impedance loads. The comparator can be separately powered down to conserve power. This comparator is used in clock generator applications to square up the filtered sine wave generated by the DDS.

Power-Down—Several individual stages may be powered down to reduce power consumption via the programming registers while still maintaining functionality of desired stages. These stages are identified in Table 7, Address 1D hex. Power-down is achieved by setting the specified bits to logic high. A logic low indicates that the stages are powered up.

Furthermore, and perhaps most significantly, the inverse sinc filters and the digital multiplier stages, can be bypassed to achieve significant power reduction through programming of the control registers in Address 20 hex. Again, logic high causes the stage to be bypassed. Of particular importance is the inverse sinc filter; this stage consumes a significant amount of power.

A full power-down occurs when all four PD bits in Control Register 1D hex are set to logic high. This reduces power consumption to approximately 10 mW (3 mA).

.

Table 6. REFCLK Multiplier Control Register Values

Mult Value	Ref Mult Bit 4	Ref Mult Bit 3	Ref Mult Bit 2	Ref Mult Bit 1	Ref Mult Bit 0
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0

PROGRAMMING THE AD9854

The AD9854 register layout, shown in Table 7, contains the information that programs the chip for the desired functionality. While many applications require very little programming to configure the AD9854, some make use of all 12 accessible register banks. The AD9854 supports an 8-bit parallel I/O operation or an SPI-compatible serial I/O operation. All accessible registers can be written and read back in either I/O operating mode.

S/P SELECT, Pin 70, is used to configure the I/O mode. Systems that use the parallel I/O mode must connect the S/P SELECT pin to V_{DD}. Systems that operate in the serial I/O mode must tie the S/P SELECT pin to GND.

Regardless of mode, the I/O port data is written to a buffer memory that does NOT affect operation of the part until the contents of the buffer memory are transferred to the register banks. The transfer of information occurs synchronously to the system clock in one of two ways:

1. Internally, at a rate programmable by the user.
2. Externally, by the user. I/O operations can occur in the absence of REFCLK but the data cannot be moved from the buffer memory to the register bank without REFCLK. See the Internal and External Update Clock section of this document for detail.

Master RESET—Logic high active, must be held high for a minimum of 10 system clock cycles. This causes the communications bus to be initialized and to load the default values listed in the Internal and External Update Clock section.

Table 7. Register Layout

Parallel Address	Serial Address	AD9854 Register Layout								
Hex	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
00	0	Phase Adjust Register No. 1 <13:8> (Bits 15, 14, don't care)					Phase 1			00h
01		Phase Adjust Register No. 1 <7:0>								00h
02	1	Phase Adjust Register No. 2 <13:8:> (Bits 15, 14, don't care)					Phase 2			00h
03		Phase Adjust Register No. 2 <7:0>								00h
04	2	Frequency Tuning Word 1 <47:40>					Frequency 1			00h
05		Frequency Tuning Word 1 <39:32>								00h
06		Frequency Tuning Word 1 <31:24>								00h
07		Frequency Tuning Word 1 <23:16>								00h
08		Frequency Tuning Word 1 <15:8>								00h
09		Frequency Tuning Word 1 <7:0>								00h
0A	3	Frequency Tuning Word 2 <47:40>					Frequency 2			
0B		Frequency Tuning Word 2 <39:32>								00h
0C		Frequency Tuning Word 2 <31:24>								00h
0D		Frequency Tuning Word 2 <23:16>								00h
0E		Frequency Tuning Word 2 <15:8>								00h
0F		Frequency Tuning Word 2 <7:0>								00h
10	4	Delta Frequency Word <47:40>								00h
11		Delta Frequency Word <39:32>								00h
12		Delta Frequency Word <31:24>								00h
13		Delta Frequency Word <23:16>								00h
14		Delta Frequency Word <15:8>								00h
15		Delta Frequency Word <7:0>								00h
16	5	Update Clock <31:24>								00h
17		Update Clock <23:16>								00h
18		Update Clock <15:8>								00h
19		Update Clock <7:0>								40h
1A	6	Ramp Rate Clock <19:16> (Bits 23, 22, 21, 20, don't care)								00h
1B		Ramp Rate Clock <15:8>								00h
1C		Ramp Rate Clock <7:0>								00h

Parallel Address	Serial Address	AD9854 Register Layout								
Hex	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
1D	7	Don't Care CR [31]	Don't Care	Don't Care	Comp PD	Reserved, Always Low	QDAC PD	DAC PD	DIG PD	10h
1E		Don't Care	PLL Range	Bypass PLL	Ref Mult 4	Ref Mult 3	Ref Mult 2	Ref Mult 1	Ref Mult 0	64h
1F		CLR ACC 1	CLR ACC 2	Triangle	SRC QDAC	Mode 2	Mode 1	Mode 0	INT/EXT Update Clk	01h
20		Don't Care	Bypass Inv Sinc	OSK EN	OSK INT	Don't Care	Don't Care	LSB First	SDO Active CR [0]	20h
21	8	Output Shape Key I Mult <11:8> (Bits 15, 14, 13, 12 don't care)								00h
22		Output Shape Key I Mult <7:0>								00h
23	9	Output Shape Key Q Mult <11:8> (Bits 15, 14, 13, 12 don't care)								00h
24		Output Shape Key Q Mult <7:0>								00h
25	A	Output Shape Key Ramp Rate <7:0>								80h
26	B	QDAC <11:8> (Bits 15, 14, 13, 12 don't care)								00h
27		QDAC <7:0> (Data is required to be in twos complement format)								0

PARALLEL I/O OPERATION

With the S/P SELECT pin tied high, the parallel I/O mode is active. The I/O port is compatible with industry-standard DSPs and microcontrollers. Six address bits, eight bidirectional data bits, and separate write/read control inputs make up the I/O port pins.

Parallel I/O operation allows write access to each byte of any register in a single I/O operation up to 1/10.5 ns. Readback capability for each register is included to ease designing with the AD9854. (Reads are not guaranteed at 100 MHz, as they are intended for software debugging only.)

Parallel I/O operation timing diagrams are shown in Figure 52 and Figure 53.

SERIAL PORT I/O OPERATION

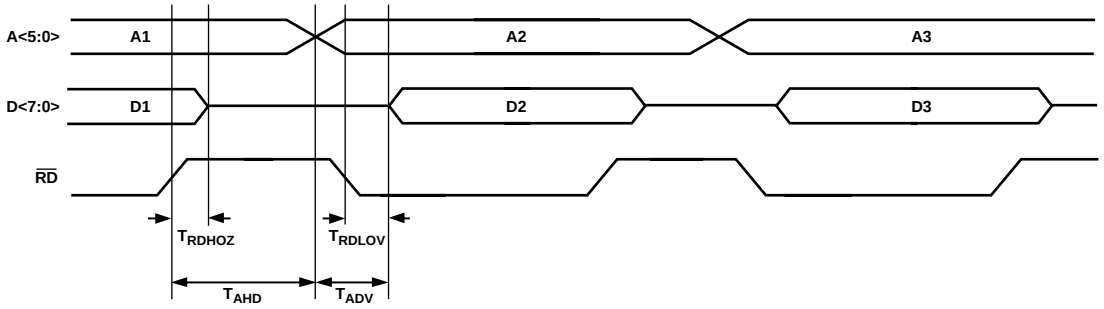
With the S/P SELECT pin tied low, the serial I/O mode is active. The serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola® 6905/11 SPI and Intel® 8051 SSR protocols. The interface allows read/write access to all 12 registers that configure the AD9854 and can be configured as a single-pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO). Data transfers are supported in most significant bit (MSB) first format or least significant bit (LSB) first format at up to 10 MHz.

When configured for serial I/O operation, most AD9854 parallel port pins are inactive; some are used for the serial I/O. Table 8 describes pin requirements for serial I/O.

Note that when operating in serial I/O mode, it is best to use the external I/O update clock mode to avoid an I/O update CLK during a serial communication cycle. Such an occurrence could cause incorrect programming due to partial data transfer. To exit the default internal update mode, program the device for external update operation at power-up, before starting the REFCLK signal, but after a master reset. Starting the REFCLK causes this information to transfer to the register bank, putting the device in external update mode.

Table 8. Serial I/O Pin Requirements

Pin Number	Pin Name	Serial I/O Description
1, 2, 3, 4, 5, 6, 7, 8	D[7:0]	The parallel data pins are not active; tie to VDD or GND.
14, 15, 16	A[5:3]	The parallel address Pins A5, A4, A3 are not active; tie to VDD or GND.
17	A2	IO RESET.
18	A1	SDO.
19	A0	SDIO.
20	I/O UD CLOCK	Update Clock. Same functionality for serial mode as parallel mode.
21	$\overline{WR}$	SCLK.
22	$\overline{RD}$	$\overline{CS}$—Chip Select



SPECIFICATION	VALUE	DESCRIPTION
T_{ADV}	15ns	ADDRESS TO DATA VALID TIME (MAXIMUM)
T_{AHD}	5ns	ADDRESS HOLD TIME TO RD SIGNAL INACTIVE (MINIMUM)
T_{RDLOV}	15ns	$\overline{RD}$ LOW TO OUTPUT VALID (MAXIMUM)
T_{RDHOZ}	10ns	$\overline{RD}$ HIGH TO DATA THREE-STATE (MAXIMUM)

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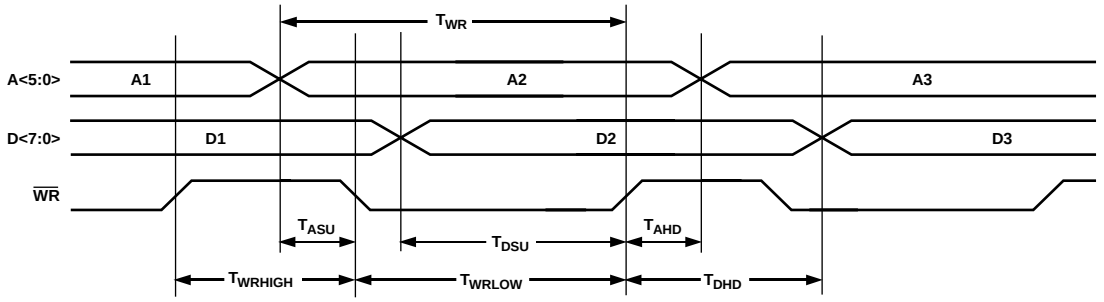
Figure 52. Parallel Port Read Timing Diagram



SPECIFICATION	VALUE	DESCRIPTION
T_{ASU}	8.0ns	ADDRESS SETUP TIME TO $\overline{WR}$ SIGNAL ACTIVE
T_{DSU}	3.0ns	DATA SETUP TIME TO $\overline{WR}$ SIGNAL ACTIVE
T_{ADH}	0ns	ADDRESS HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE
T_{DHD}	0ns	DATA HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE
T_{WRLOW}	2.5ns	$\overline{WR}$ SIGNAL MINIMUM LOW TIME
T_{WRHIGH}	7ns	$\overline{WR}$ SIGNAL MINIMUM HIGH TIME
T_{WR}	10.5ns	MINIMUM WRITE TIME

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Figure 53. Parallel Port Write Timing Diagram

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a serial communication cycle with the AD9854. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9854, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9854 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, and the register address to be acted upon.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9854. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9854 and the system controller. The number of data bytes transferred in Phase 2 of the communication cycle is a function of the register address. (Table 9 describes how many bytes must be transferred.) The AD9854 internal serial I/O controller expects every byte of the register being accessed to be transferred. Thus, the user would want to write between I/O update clocks.

At the completion of any communication cycle, the AD9854 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle. In addition, an active high input on the IO RESET pin immediately terminates the current communication cycle. After IO RESET returns low, the AD9854 serial port controller requires the next eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9854 is registered on the rising edge of SCLK. All data is driven out of the AD9854 on the falling edge of SCLK.

Figure 54 and Figure 55 show the general operation of the AD9854 serial port.

Table 9. Register Address vs. Data Bytes Transferred

Serial Register Address	Register Name	Bytes Transferred
0	Phase Offset Tuning Word Register No. 1	2
1	Phase Offset Tuning Word Register No. 2	2
2	Frequency Tuning Word No. 1	6
3	Frequency Tuning Word No. 2	6
4	Delta Frequency Register	6
5	Update Clock Rate Register	4
6	Ramp Rate Clock Register	3
7	Control Register	4
8	I Path Digital Multiplier Register	2
9	Q Path Digital Multiplier Register	2
A	Shaped On/Off Keying Ramp Rate Register	1
B	Q DAC Register	2

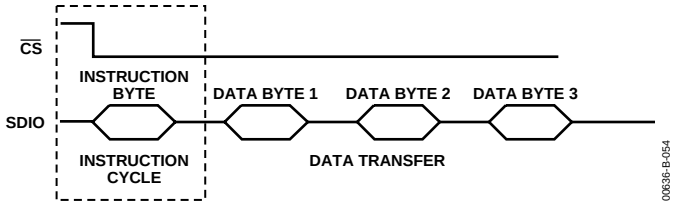

Figure 54. Using SDIO as a Read/Write Transfer

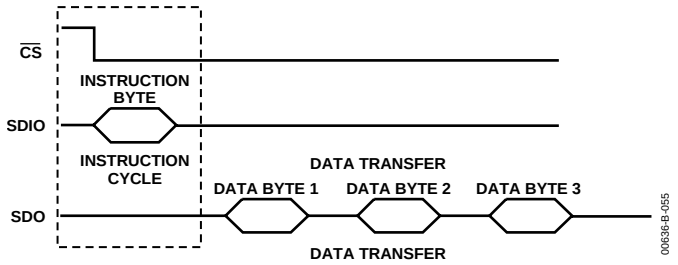

Figure 55. Using SDIO as an Input, SDO as an Output

INSTRUCTION BYTE

The instruction byte contains the following information.

Table 10. Instruction Byte Information

MSB	D6	D5	D4	D3	D2	D1	LSB
R/$\overline{W}$	X	X	X	A3	A2	A1	A0

R/$\overline{W}$—Bit 7 determines whether a read or write data transfer occurs following the instruction byte. Logic high indicates read operation. Logic 0 indicates a write operation.

Bits 6, 5, and 4 are dummy bits (don't care).

A3, A2, A1, A0—Bits 3, 2, 1, and 0 determine which register is accessed during the data transfer portion of the communications cycle. See Table 7 for register address details.

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK

Serial Clock (Pin 21). The serial clock pin is used to synchronize data to and from the AD9854 and to run the internal state machines. SCLK maximum frequency is 10 MHz.

$\overline{CS}$

Chip Select (Pin 22). Active low input that allows more than one device on the same serial communications line. The SDO and SDIO pins go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until $\overline{CS}$ is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

SDIO

Serial Data I/O (Pin 19). Data is always written to the AD9854 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 0 of Register Address 20h. The default is Logic 0, which configures the SDIO pin as bidirectional.

SDO

Serial Data Out (Pin 18). Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9854 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

IO RESET

Synchronize I/O Port (Pin 17). Synchronizes the I/O port state machines without affecting the contents of the addressable registers. An active high input on the IO RESET pin causes the current communication cycle to terminate. After IO reset returns low (Logic 0), another communication cycle may begin, starting with the instruction byte.

NOTES ON SERIAL PORT OPERATION

The AD9854 serial port configuration bits reside in Bit 1 and Bit 0 of Register Address 20h. It is important to note that the configuration changes immediately upon a valid I/O update. For multibyte transfers, writing to this register may occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remainder of the current communication cycle.

The system must maintain synchronization with the AD9854, or the internal control logic is not able to recognize further instructions. For example, if the system sends the instruction to write a 2-byte register, then pulses the SCLK pin for a 3-byte register (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle will properly write the first two data bytes into the AD9854, but the next eight rising SCLK edges are interpreted as the next instruction byte, not the final byte of the previous communication cycle.

In the case where synchronization is lost between the system and the AD9854, the IO RESET pin provides a means to reestablish synchronization without reinitializing the entire chip. Asserting the IO RESET pin (active high) resets the AD9854 serial port state machine, terminating the current I/O operation and putting the device into a state in which the next eight SCLK rising edges are understood to be an instruction byte. The IO RESET pin must be deasserted (low) before the next instruction byte write can begin. Any information that is written to the AD9854 registers during a valid communication cycle prior to loss of synchronization remains intact.

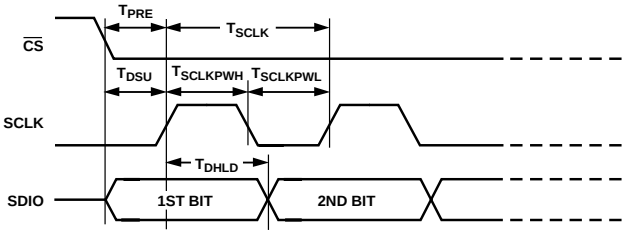

Figure 56. Timing Diagram for Data Write to AD9854

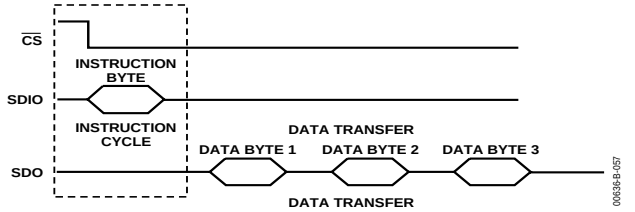

Figure 57. Timing Diagram for Read from AD9854

MSB/LSB TRANSFERS

The AD9854 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by Bit 1 of Serial Register Bank 20h. When this bit is set active high, the AD9854 serial port is in LSB-first format. This bit defaults low, to the MSB-first format. The instruction byte must be written in the format indicated by Bit 1 of Serial Register Bank 20h. That is, if the AD9854 is in LSB-first mode, the instruction byte must be written from least significant bit to most significant bit.

CONTROL REGISTER DESCRIPTION

The control register is located in the shaded portion of Table 7 at Address 1D through 20 hex. It is composed of 32 bits. Bit 31 is located at the top left position and Bit 0 is located in the lower right position of the shaded portion. In the text that follows, the register descriptions have been subdivided to make it easier to locate the text associated with specific control categories.

CR[31:29] are open.

CR[28] is the comparator power-down bit. When this bit is set (Logic 1), its signal tells the comparator that a power-down mode is active. This bit is an output of the digital section and is an input to the analog section.

CR[27] must always be written to Logic 0. Writing this bit to Logic 1 causes the AD9854 to stop working until a master reset is applied.

CR[26] is the Q DAC power-down bit. When this bit is set (Logic 1), it tells the Q DAC that a power-down mode is active.

CR[25] is the full DAC power-down bit. When this bit is set (Logic 1), it tells both the I and Q DACs, as well as the reference, that a power-down mode is active.

CR[24] is the digital power-down bit. When this bit is set (Logic 1), this signal indicates to the digital section that a power-down mode is active. Within the digital section, the clocks are forced to dc, effectively powering down the digital section. The PLL still accepts the REFCLK signal and continues to output the higher frequency.

CR[23] is reserved. Write to zero.

CR[22] is the PLL range bit, which controls the VCO gain. The power-up state of the PLL range bit is Logic 1, higher gain for frequencies above 200 MHz.

CR[21] is the bypass PLL bit, active high. When this bit is active, the PLL is powered down and the REFCLK input is used to drive the system clock signal. The power-up state of the bypass PLL bit is Logic 1, PLL bypassed.

CR[20:16] bits are the PLL multiplier factor. These bits are the REFCLK multiplication factor, unless the bypass PLL bit is set. The PLL multiplier valid range is from 4 to 20, inclusive.

CR[15] is the Clear Accumulator 1 bit. This bit has a one-shot type function. When this bit is written active, Logic 1, a Clear Accumulator 1 signal is sent to the DDS logic, resetting the accumulator value to zero. The bit is then automatically reset, but the buffer memory is not reset. This bit allows the user to easily create a saw-toothed frequency sweep pattern with minimal intervention. This bit is intended for chirp mode only, but its function is still retained in other modes.

CR[14] is the clear accumulator bit. This bit, active high, holds both the Accumulator 1 and Accumulator 2 values at zero for as long as the bit is active. This allows the DDS phase to be initialized via the I/O port.

CR[13] is the triangle bit. When this bit is set, the AD9854 automatically performs a continuous frequency sweep from F1 to F2 frequencies and back. The effect is a triangular frequency sweep. When this bit is set, the operating mode must be set to ramped FSK.

CR[12] is the source Q DAC bit. When this bit is set high, the Q path DAC accepts data from the Q DAC register.

CR[11:9] are the three bits that describe the five operating modes of the AD9854:

0h = Single-Tone mode
1h = FSK mode
2h = Ramped FSK mode
3h = Chirp mode
4h = BPSK mode

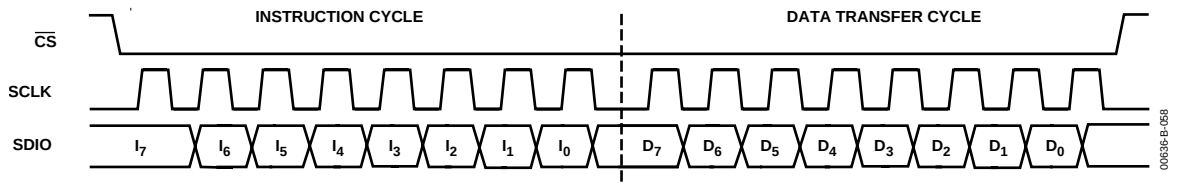

Figure 58. Serial Port Write Timing-Clock Stall low

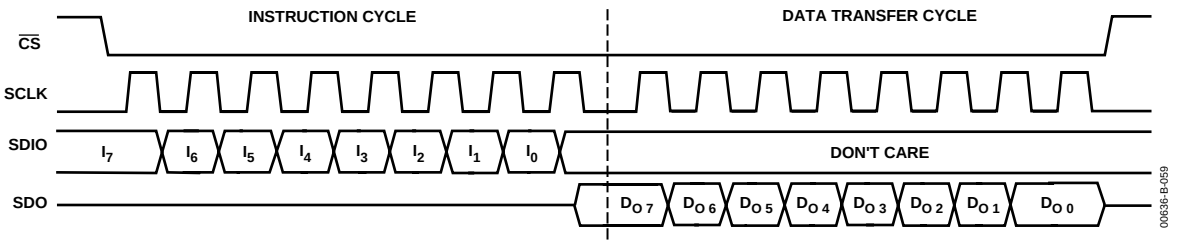

Figure 59. 3-Wire Serial Port Read Timing-Clock Stall Low

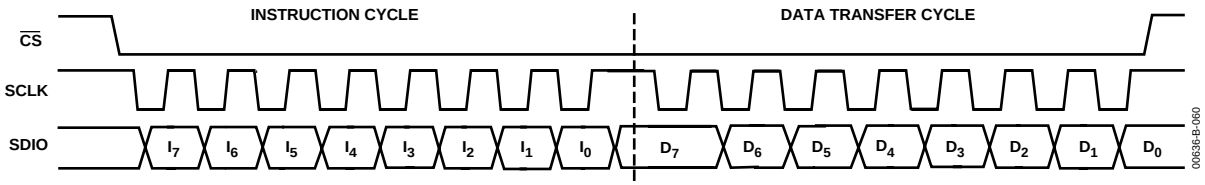

Figure 60. Serial Port Write Timing-Clock Stall High

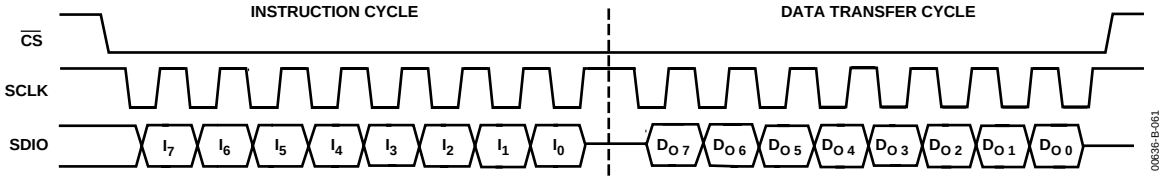

Figure 61. 2-Wire Serial Port Read Timing-Clock Stall High

CR[8] is the internal update active bit. When this bit is set to Logic 1, the I/O UD CLK pin is an output and the AD9854 generates the I/O UD CLK signal. When set to Logic 0, external I/O UD CLK functionality is performed and the I/O UD CLK pin is configured as an input.

CR[7] is reserved. Write to zero.

CR[6] is the inverse sinc filter bypass bit. When this bit is set, the data from the DDS block goes directly to the output shaped-keying logic and the clock to the inverse sinc filter is stopped. Default is clear, filter enabled.

CR[5] is the shaped-keying enable bit. When this bit is set, the output ramping function is enabled and is performed in accordance with the CR[4] bit requirements.

CR[4] is the internal/external output shaped-keying control bit. When this bit is set to Logic 1, the shaped-keying factor is internally generated and applied to both the I and Q paths. When cleared (default), the output shaped-keying function is externally controlled by the user and the shaped-keying factor is the I and Q output shaped-keying factor register value. The two registers that are the shaped-keying factors also default low such that the output is off at power-up and until the device is programmed by the user.

CR[3:2] are reserved. Write to zero.

CR[1] is the serial port MSB/LSB first bit. Defaults low, MSB first.

CR[0] is the serial port SDO active bit. Defaults low, inactive.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The AD9854 is a multifunctional, high speed device that targets a wide variety of synthesizer and agile clock applications. The numerous innovative features contained in the device each consume incremental power. If enabled in combination, the safe thermal operating conditions of the device may be exceeded. Careful analysis and consideration of power dissipation and thermal management is a critical element in the successful application of the AD9854 device.

The AD9854 device is specified to operate within the industrial temperature range of −40°C to +85°C. This specification is conditional, however, such that the absolute maximum junction temperature of 150°C is not exceeded. At high operating temperatures, extreme care must be taken in the operation of the device to avoid exceeding the junction temperature, which results in a potentially damaging thermal condition.

Many variables contribute to the operating junction temperature within the device, including:

- Package style
- Selected mode of operation
- Internal system clock speed
- Supply voltage
- Ambient temperature

The combination of these variables determines the junction temperature within the AD9854 for a given set of operating conditions.

The AD9854 is available in two package styles: a thermally enhanced, surface-mount package with an exposed heat sink, and a nonthermally enhanced, surface-mount package. The thermal impedance of these packages is 16°C/W and 38°C/W, respectively, measured under still-air conditions.

THERMAL IMPEDANCE

The thermal impedance of a package can be thought of as a thermal resistor that exists between the semiconductor surface and the ambient air. The thermal impedance is determined by the package material and the physical dimensions of the package. The dissipation of the heat from the package is directly dependent upon the ambient air conditions and the physical connection made between the IC package and the PCB. Adequate dissipation of power from the AD9854 relies on all power and ground pins of the device being soldered directly to a copper plane on a PCB. In addition, the thermally enhanced package of the AD9854ASQ contains a heat sink on the bottom of the package that must be soldered to a ground pad on the PCB surface. This pad must be connected to a large copper plane which, for convenience, may be a ground plane. Sockets for either package style of the device are not recommended.

JUNCTION TEMPERATURE CONSIDERATIONS

The power dissipation (P_{DISS}) of the AD9854 in a given application is determined by many operating conditions. Some of the conditions have a direct relationship with P_{DISS}, such as supply voltage and clock speed, but others are less deterministic. The total power dissipation within the device, and its effect on the junction temperature, must be considered when using the device. The junction temperature of the device is given by

(Thermal Impedance × Power Consumption) + Ambient Temperature.

Given that the junction temperature should never exceed 150°C, and that the ambient temperature can be 85°C, the maximum power consumption for the AD9854AST is 1.7 W and 4.1 W for the AD9854ASQ (thermally-enhanced package). Factors affecting the power dissipation follow.

Supply Voltage

The supply voltage affects power dissipation and junction temperature because P_{DISS} equals V × I. Users should design for 3.3 V nominal; however, the device is guaranteed to meet specifications over the full temperature range and over the supply voltage range of 3.135 V to 3.465 V.

Clock Speed

Clock speed directly and linearly influences the total power dissipation of the device, and, therefore, junction temperature. As a rule, to minimize power dissipation, the user should always select the lowest internal clock speed possible to support a given application. Typically, the usable frequency output bandwidth from a DDS is limited to 40% of the clock rate to keep reasonable requirements on the output low-pass filter. For the typical DDS application, the system clock frequency should be 2.5× the highest desired output frequency.

Mode of Operation

The selected operational mode of operation of the AD9854 has a great influence on the total power consumption. The AD9854 offers many features and modes, each of which imposes an additional power requirement. Though the collection of features contained in the AD9854 target a wide variety of applications, the device was designed under the assumption that only a few features would be enabled for any given application. In fact, enabling multiple features at higher clock speeds may cause the maximum junction temperature of the die to be exceeded. This can severely limit the long-term reliability of the device. Figure 62 and Figure 63 show the power requirements associated with the individual features of the AD9854. These graphs should be used as a guide in determining the optimum application of the AD9854 for reliable operation.

As can be seen in Figure 63, the inverse sinc filter function requires a significant amount of power. As an alternate approach to maintaining flatness across the output bandwidth, the digital multiplier function may be used to adjust the output signal level, at a dramatic savings in power consumption. Careful planning and management of the feature set minimizes power dissipation and avoids exceeding junction temperature requirements within the IC.

Figure 62 shows the supply current consumed by the AD9854 over a range of frequencies for two possible configurations. All circuits enabled means the output scaling multipliers, the inverse sinc filter, the Q DAC, and the on-board comparator are all enabled, while basic configuration means the output scaling multipliers, the inverse sinc filter, the Q DAC, and the on-board comparator are all disabled.

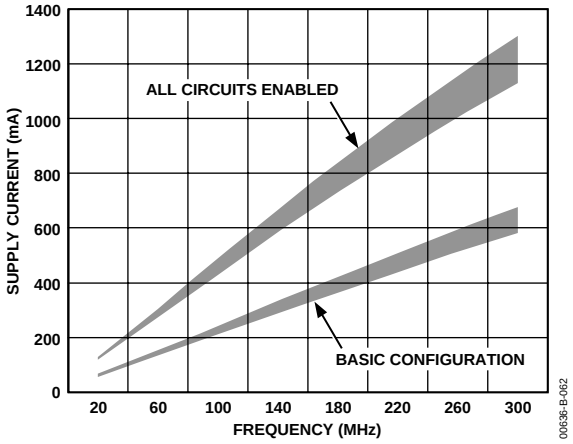

Figure 62. Current Consumption vs. Clock Frequency

Figure 63 shows the approximate current consumed by each of four functions.

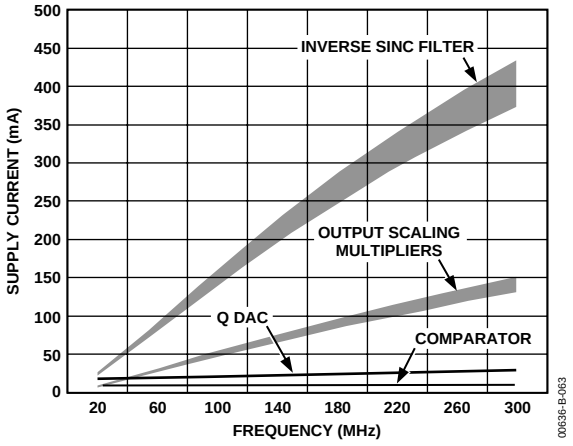

Figure 63. Current Consumption by Function vs. Clock frequency

EVALUATION OF OPERATING CONDITIONS

The first step in applying the AD9854 is to select the internal clock frequency. Clock frequency selections above 200 MHz require the use of the thermally enhanced package (AD9854ASQ); clock frequency selections of 200 MHz and below may allow the use of the standard plastic surface-mount package, but more information is needed to make that determination.

The second evaluation step is to determine the maximum required operating temperature for the AD9854 in the given application. Subtract this value from 150°C, which is the maximum junction temperature allowed for the AD9854. For the extended industrial temperature range, the maximum operating temperature is 85°C, which results in a difference of 65°C. This is the maximum temperature gradient that the device may experience due to power dissipation.

The third evaluation step is to divide this maximum temperature gradient by the thermal impedance, to arrive at the maximum power dissipation allowed for the application. For the example so far, 65°C divided by both versions of the AD9854 packages' thermal impedances of 38°C/W and 16°C/W, respectively, yields a total power dissipation limit of 1.7 W and 4.1 W, respectively. This means that for a 3.3 V nominal power supply voltage, the current consumed by the device under full operating conditions must not exceed 515 mA in the standard plastic package and 1242 mA in the thermally enhanced package. The total set of enabled functions and operating conditions of the AD9854 application must support these current consumption limits.

To determine the suitability of a given AD9854 application vs. the power dissipation requirements, use Figure 62 and Figure 63. These graphs assume that the AD9854 device is soldered to a multilayer PCB per the recommended best manufacturing practices and procedures for the given package type. This ensures that the specified thermal impedance specifications are achieved.

THERMALLY ENHANCED PACKAGE MOUNTING GUIDELINES

This section provides general recommendations for mounting the AD9854ASQ (the thermally enhanced exposed heat sink package) to printed circuit boards. The exceptional thermal characteristics of this package depend entirely upon proper mechanical attachment.

Figure 64 shows the package from the bottom and the dimensions of the exposed heat sink. A solid conduit of solder must be established between this pad and the surface of the PCB.

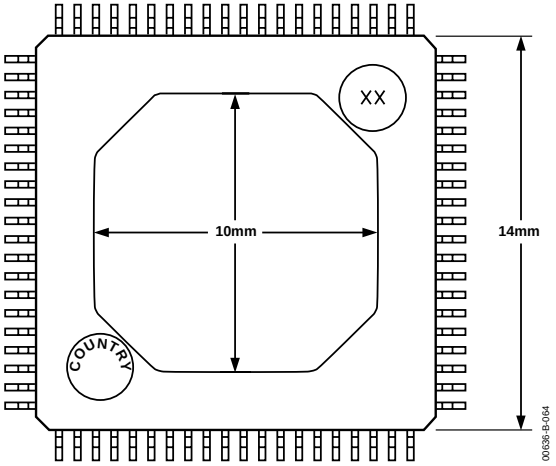

Figure 64. Package Bottom and Exposed Heat Sink

Figure 65 depicts a general PCB land pattern for an exposed heat sink device. Note that this pattern is for a 64-lead device, not an 80-lead, but the relative shapes and dimensions still apply. In this land pattern, a solid copper plane exists inside the individual lands for device leads. Also, the solder mask opening is conservatively dimensioned to avoid any assembly problems.

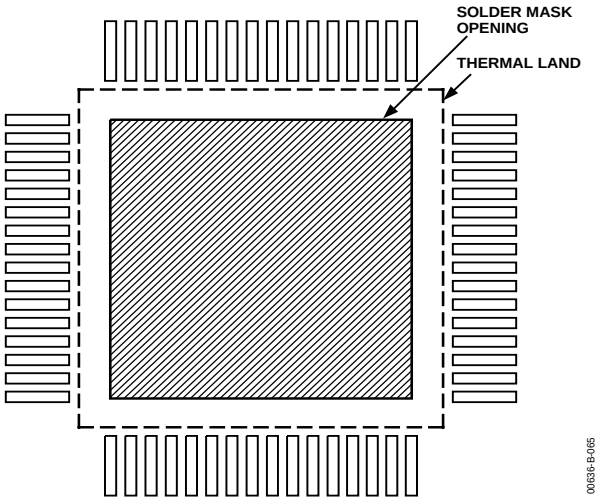

Figure 65. General PCB Land Pattern

The thermal land itself must be able to distribute heat to an even larger copper plane such as an internal ground plane. Vias must be uniformly provided over the entire thermal pad to connect to this internal plane. A proposed via pattern is shown in Figure 66. Via holes should be small (12 mils, 0.3 mm) such that they can be plated and plugged. These provide the mechanical conduit for heat transfer.

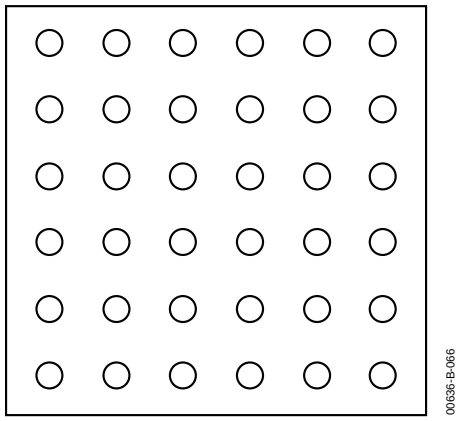

Figure 66. Proposed Via Pattern

Finally, a proposed stencil design is shown in Figure 67 for screen solder placement. Note that if vias are not plugged, wicking occurs, which displaces solder away from the exposed heat sink, and the necessary mechanical bond is not established.

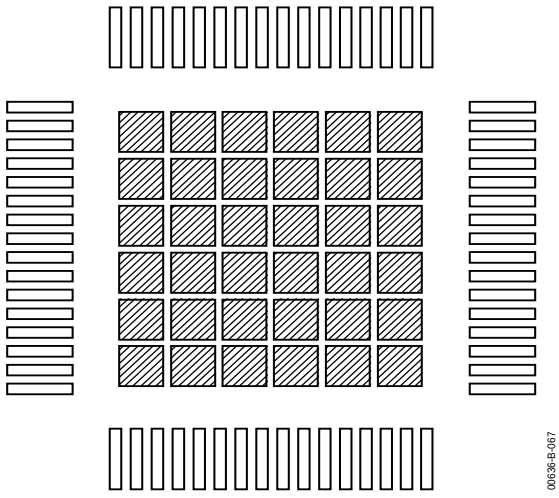

Figure 67. Proposed Stencil Design for Screen Solder Placement

EVALUATION BOARD

An evaluation board package is available for AD9854 DDS devices. This package consists of a PCB, software, and documentation to facilitate bench analysis of the device's performance. To ensure optimum dynamic performance from the device, it is recommended that AD9854 users familiarize themselves with the operation and performance capabilities of the device with the evaluation board and use the evaluation board as a PCB reference design.

EVALUATION BOARD INSTRUCTIONS

The AD9852/AD9854 Revision E evaluation board includes either an AD9852ASQ or AD9854ASQ IC.

The ASQ package permits 300 MHz operation by virtue of its thermally enhanced design. This package has a bottom-side heat slug that must be soldered to the ground plane of the PCB directly beneath the IC. In this manner, the evaluation board PCB ground plane layer extracts heat from the AD9852/AD9854 IC package. If device operation is limited to 200 MHz and below, the AST package without a heat slug may be used in customer installations over the full temperature range. The AST package is less expensive than the ASQ package and those costs are reflected in the price of the IC.

Evaluation boards for both the AD9852 and AD9854 are identical except for the installed IC.

To assist in proper placement of the pin header shorting-jumpers, the instructions refer to direction (left, right, top, bottom) as well as header pins to be shorted. Pin 1 for each 3-pin header has been marked on the PCB corresponding with the schematic diagram. When following these instructions, position the PCB so that the PCB text can be read from left to right. The board is shipped with the pin headers configuring the board as follows:

- REFCLK for the AD9852/AD9854 is configured as differential. The differential clock signals are provided by the MC100LVEL16D differential receiver.
- Input clock for the MC100LVEL16D is single-ended via J25. This signal may be 3.3 V CMOS or a 2 V p-p sine wave capable of driving 50 Ω (R13).
- Both DAC outputs from the AD9852/AD9854 are routed through the two 120 MHz elliptical LP filters and their outputs connected to J7 (Q or Control DAC) and J6 (I or Cosine DAC).
- The board is set up for software control via the printer port connector.
- The DAC's output currents are configured for 10 mA.

GENERAL OPERATING INSTRUCTIONS

Load the CD software on your PC's hard disk. The current software (Version 1.72) supports Windows® 95, Windows 98, Windows 2000, Windows NT®, and Windows XP.

Connect a printer cable from the PC to the AD9854 evaluation board printer port connector labeled J11.

Hardware preparation: Use the schematic in conjunction with these instructions to become acquainted with the electrical functioning of the evaluation board.

Attach power wires to connector labeled TB1 using the screw-down terminals. This is a plastic connector that press-fits over a 4-pin header soldered to the board. Table 11 shows connections to each pin. DUT = device under test.

Table 11. Power Requirements for DUT Pins

AVDD 3.3 V	DVDD 3.3 V	VCC 3.3 V	Ground
For all DUT analog pins	For all DUT digital pins	For all other devices	For all devices

Attach REFCLK to the clock input, J25.

Clock Input, J25

This is a single-ended input that, for conversion to differential PECL output, is routed to the MC100LVEL16D. This is accomplished by attaching a 2 V p-p clock or sine wave source to J25. Note that this is a 50 Ω impedance point set by R13. The input signal is ac-coupled and then biased to the center-switching threshold of the MC100LVEL16D. To engage the differential clocking mode of the AD9854, W3 Pins 2 and 3 (the bottom two pins) must be connected with a shorting jumper.

The signal arriving at the AD9854 is called the reference clock. When engaging the on-chip PLL clock multiplier, this signal is the reference clock for the PLL and the multiplied PLL output becomes the system clock. If the PLL clock multiplier is to be bypassed, the reference clock supplied by the user is directly operating the AD9854 and is, therefore, the system clock.

Three-State Control

Switch headers W9, W11, W12, W13, W14, and W15 must be shorted to allow the provided software to control the AD9854 evaluation board via the printer port connector J11.

Programming

If programming of the AD9854 is not to be provided by the user's PC and ADI software, Headers W9, W11, W12, W13, W14, and W15 should be opened (shorting jumpers removed). This effectively detaches the PC interface and allows the 40-pin headers, J10 and J1, to assume control without bus contention. Input signals on J10 and J1 going to the AD9854 should be 3.3 V CMOS logic levels.

Low-Pass Filter Testing

The purpose of 2-pin headers W7 and W10 (associated with J4 and J5) is to allow the two 50 Ω, 120 MHz filters to be tested during PCB assembly without interference from other circuitry attached to the filter inputs. Typically, a shorting jumper is attached to each header to allow the DAC signals to be routed to the filters. If the user wishes to test the filters, the shorting jumpers at W7 and W10 should be removed and 50 Ω test signals applied at J4 and J5 inputs to the 50 Ω elliptic filters. Users should refer to the schematic provided and the following sections to properly position the remaining shorting jumpers.

Observing the Unfiltered IOUT1 and the Unfiltered IOUT2 DAC Signals

The unfiltered DAC outputs may be observed at J5 (the I or cosine signal) and J4 (the Q or Control DAC signal). The procedure below simply routes the two 50 Ω terminated analog DAC outputs to the SMB connectors and disconnects any other circuitry. The raw DAC outputs may appear as a series of quantized (stepped) output levels that may not resemble a sine wave until they are filtered. The default 10 mA output current develops a 0.5 V p-p signal across the on-board 50 Ω termination. If the observation equipment offers 50 Ω inputs, the DAC develops only 0.25 V p-p due to the double termination.

1. Install shorting jumpers at W7 and W10.
2. Remove shorting jumper at W16.
3. Remove shorting jumper from 3-pin header W1.
4. Install shorting jumper on Pins 1 and 2 (bottom two pins) of 3-pin header W4.

On the AD9852 evaluation board, IOUT2, the control DAC output, is under user control through the serial or parallel ports. The 12-bit, twos complement value(s) is/are written to the control DAC register that sets the IOUT2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum) with all zeros being midscale. Rapidly changing the contents of the control DAC register (up to 100 MSPS) allows IOUT2 to assume any waveform that can be programmed.

Observing the Filtered IOUT1 and the Filtered IOUT2

The filtered I and Q (or control) DAC outputs may be observed at J6 (the I signal) and J7 (the Q or control signal). This places the 50 Ω (input and output Z) low-pass filters in the I and Q (or control) DAC pathways to remove images and aliased harmonics and other spurious signals above approximately 120 MHz. These I and Q signals appear as nearly pure sine waves and 90° out of phase with each other. These filters are designed with the assumption that the system clock speed is at or near maximum (300 MHz). If the system clock speed is much less than 300 MHz, for example 200 MHz, it is possible or inevitable that unwanted DAC products other than the fundamental signal are passed by the low-pass filters.

If the AD9852 evaluation board is used, any reference to the Q signal should be interpreted to mean the control DAC.

1. Install shorting jumpers at W7 and W10.
2. Install shorting jumper at W16.
3. Install shorting jumper on Pins 1 and 2 (bottom two pins) of 3-pin header W1.
4. Install shorting jumper on Pins 1 and 2 (bottom two pins) of 3-pin header W4.
5. Install shorting jumper on Pins 2 and 3 (bottom two pins) of 3-pin header W2 and W8.

Observing the Filtered IOUT1 and the Filtered $\overline{IOUT1}$

The filtered I DAC outputs may be observed at J6 (the true signal) and J7 (the complementary signal). This places the 120 MHz low-pass filters in the true and complementary output paths of the I DAC to remove images and aliased harmonics and other spurious signals above approximately 120 MHz. These signals appear as nearly pure sine waves and 180 degrees out of phase with each other. If the system clock speed is much less than 300 MHz, for example 200 MHz, it is possible or inevitable that unwanted DAC products other than the fundamental signal are passed by the low-pass filters.

1. Install shorting jumpers at W7 and W10.
2. Install shorting jumper at W16.
3. Install shorting jumper on Pins 2 and 3 (top two pins) of 3-pin header W1.
4. Install shorting jumper on Pins 2 and 3 (top two pins) of 3-pin header W4.
5. Install shorting jumpers on Pins 2 and 3 (bottom two pins) of 3-pin header W2 and W8.

To Connect the High Speed Comparator

To connect the high speed comparator to the DAC output signals, either the quadrature filtered output configuration (AD9854 only) or the complementary filtered output configuration outlined in the previous section (for both the AD9854 and the AD9852) can be chosen. Follow Steps 1 through 4 for either filtered configuration as described previously. Then install a shorting jumper on Pins 1 and 2 (top two pins) of 3-pin header W2 and W8. This reroutes the filtered signals away from their output connectors (J6 and J7) and to the 100 Ω configured comparator inputs. This sets up the comparator for differential input without control of the comparator output duty cycle. The comparator output duty cycle should be close to 50% in this configuration.

The user may elect to change the R_{SET} resistor, R2, from 3.9 kΩ to 1.95 kΩ to receive a more robust signal at the comparator inputs. This decreases jitter and extends the comparator operating range. This may be accomplished by installing a shorting jumper at W6, which provides a second 3.9 kΩ chip resistor (R20) in parallel with the provided R2. This boosts the DAC output current from 10 mA to 20 mA and doubles the peak-to-peak output voltage developed across the loads.

Single-Ended Configuration

To connect the high speed comparator in a single-ended configuration that allows duty cycle or pulse width control requires that a dc threshold voltage be present at one of the comparator inputs. The user may supply this voltage using the control DAC. A 12-bit, twos complement value is written to the control DAC register that sets the IOUT2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum) with all zeros being midscale. The IOUT1 channel continues to output a filtered sine wave programmed by the user. These two signals are routed to the comparator using W2 and W8 3-pin header switches. The configuration described in the section Observing the Filtered IOUT1 and the Filtered IOUT2 must be used. Follow Steps 1 through 4 in that section, then install shorting jumpers on Pins 1 and 2 (top two pins) of the 3-pin header W2 and W8.

The user may elect to change the R_{SET} resistor, R2, from 3.9 kΩ to 1.95 kΩ to receive a more robust signal at the comparator inputs. This decreases jitter and extends the comparator operating range. The user can accomplish this by installing a shorting jumper at W6, which provides a second 3.9 kΩ chip resistor (R20) in parallel with the provided R2.

USING THE PROVIDED SOFTWARE

The evaluation software is provided on a CD. This brief set of instructions should be used in conjunction with the AD9852 or AD9854 data sheet and the AD9852/AD9854 evaluation board schematic.

The CD contains the following:

- The AD9852/AD9854 evaluation software
- AD9854 evaluation board instructions
- AD9854 data sheet
- AD9854 evaluation board schematics
- AD9854 PCB layout

Several numerical entries, such as frequency and phase information, require users to press the Enter key to register the information. So, for example, if a new frequency is input and nothing new happens when the load button is pressed, the user probably neglected to press the Enter key after typing the new frequency information.

Normal operation of the AD9852/AD9854 evaluation board begins with a master reset. Many of the default register values after reset are depicted in the software control panel. The reset command sets the DDS output amplitude to minimum and 0 Hz, 0 phase-offset as well as other states that are listed in the AD9852/AD9854 Register Layout table in the data sheet.

The next programming block should be the reference clock and multiplier because this information is used to determine the proper 48-bit frequency tuning words that are entered and calculated later.

The output amplitude defaults to the 12-bit straight binary multiplier values of the I or cosine multiplier register of 000 hex and no output (dc) should be seen from the DAC. Set the multiplier amplitude in the Output Amplitude box to a substantial value, such as FFF hex. The digital multiplier may be bypassed by clicking the box Output Amplitude Is Always Full Scale, but experience has shown that doing so does not result in best spurious-free dynamic range (SFDR). Best SFDR, as much as 11 dB better, is obtained by routing the signal through the digital multiplier and backing off on the multiplier amplitude. For instance, FC0 hex produces less spurious signal amplitude than FFF hex. It is an exploitable and repeatable phenomenon that should be investigated in your application if SFDR must be maximized. This phenomenon is more readily observed at higher output frequencies where good SFDR becomes more difficult to achieve.

Refer to this data sheet and evaluation board schematic to understand all the functions of the AD9854 available to the user and to gain an understanding of what the software is doing in response to programming commands.

SUPPORT

Applications assistance is available for the AD9854, the AD9854 PCB evaluation board, and all other Analog Devices products. Please call 1-800-ANALOGD or visit www.analog.com.

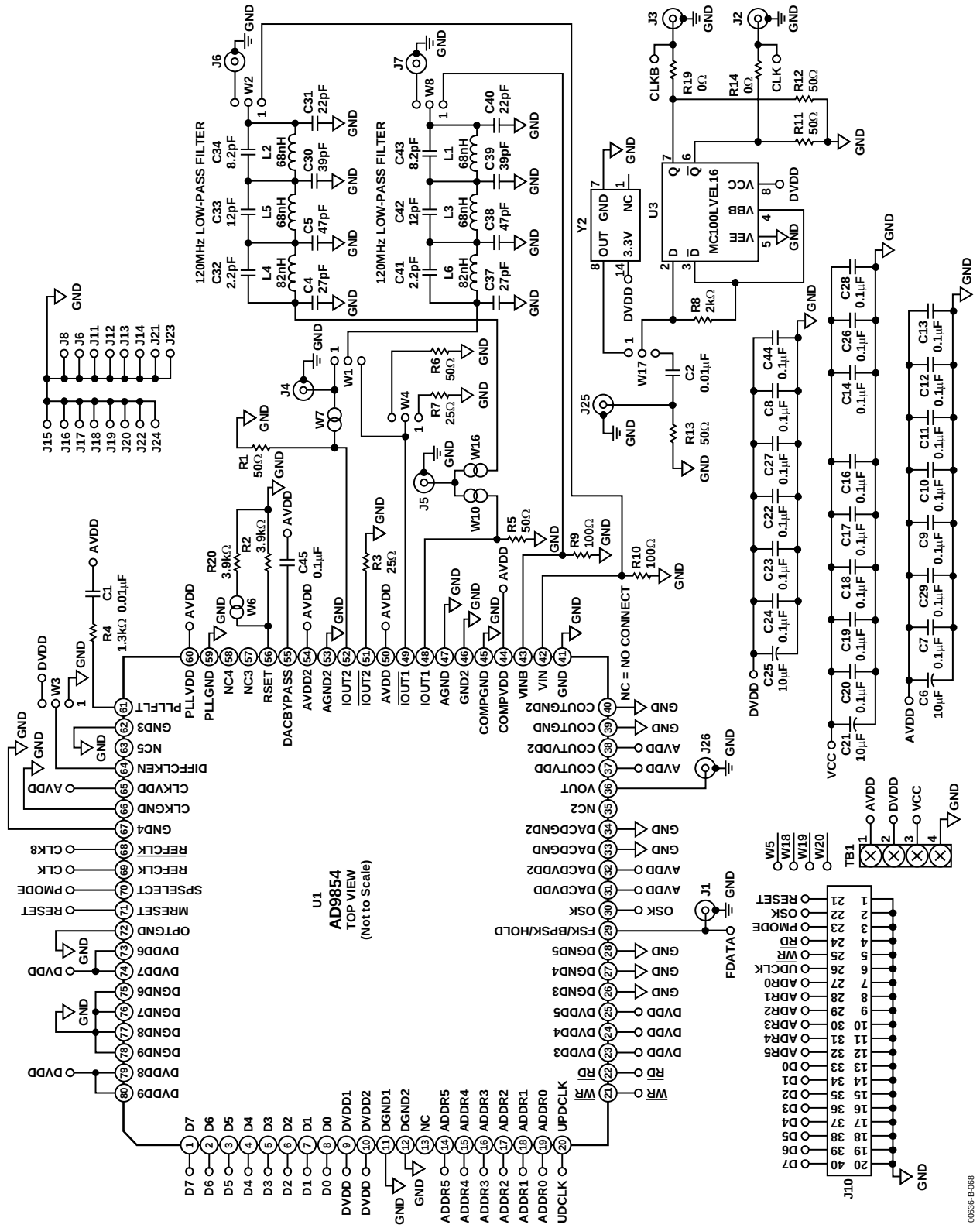

Figure 68. Evaluation Board Schematic

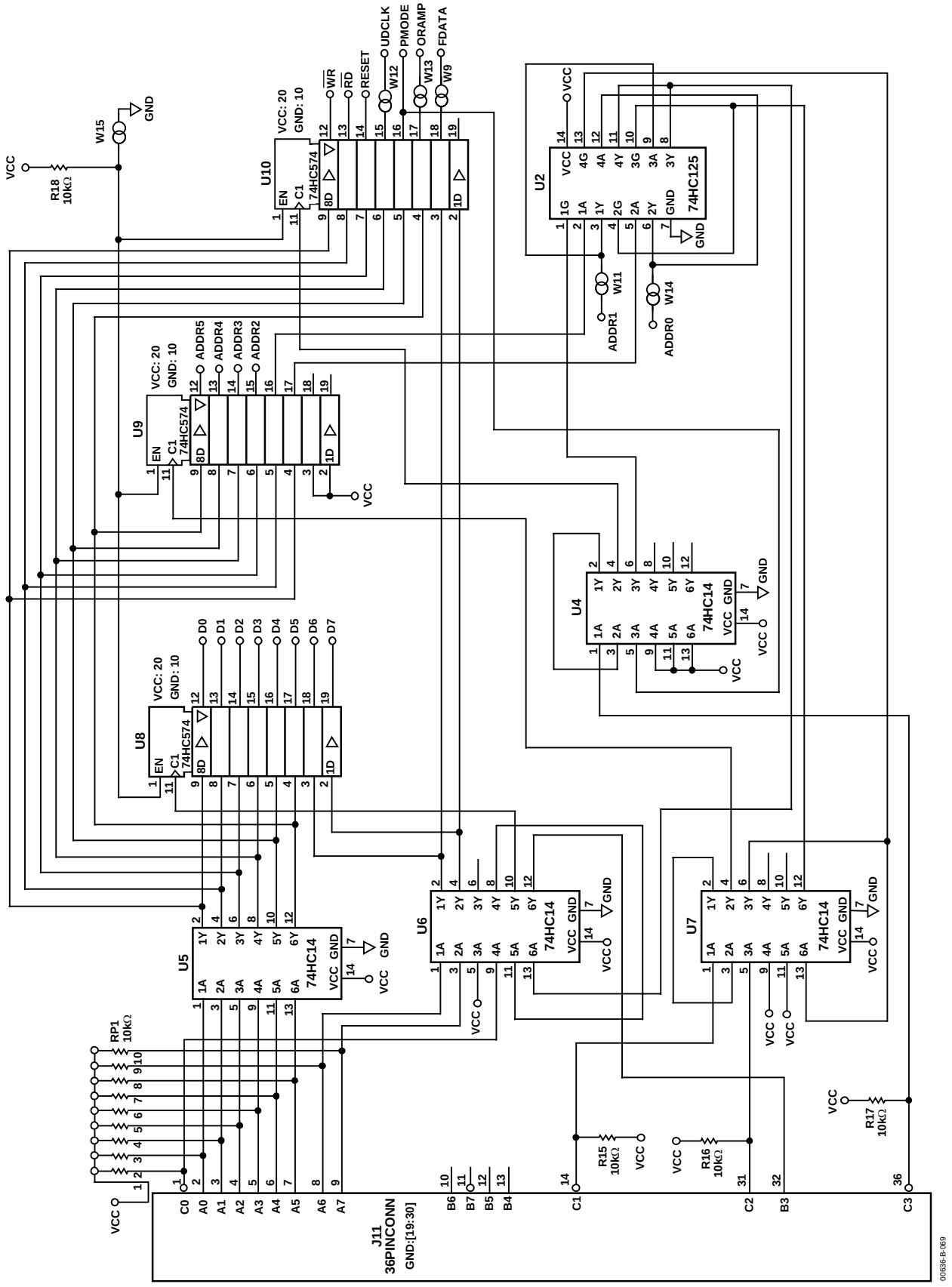

Figure 69. Evaluation Board Schematic

Table 12. AD9852/AD9854 Customer Evaluation Board (AD9852 PCB > U1 = AD9852ASQ, AD9854 PCB > U1 = AD9854ASQ)

No.	Quantity	REFDES	Device	Package	Value	Mfg. Part No.
1	3	C1, C2, C45	Capacitor	0805	0.01 µF	
2	21	C7 to C14, C16 to C20, C22 to C24, C26 to C29, C44	Capacitor	0603	0.1 µF	
3	2	C4, C37	Capacitor	1206	27 pF	
4	2	C5, C38	Capacitor	1206	47 pF	
5	3	C6, C21, C25	BCAPT	TAJD	10 µF	
6	2	C30, C39	Capacitor	1206	39 pF	
7	2	C31, C40	Capacitor	1206	22 pF	
8	2	C32, C41	Capacitor	1206	2.2 pF	
9	2	C33, C42	Capacitor	1206	12 pF	
10	2	C34, C43	Capacitor	1206	8.2 pF	
11	9	J1 to J7, J25, J26	SMB	STR-PC MNT		ITT Industries B51–351–0000220
12	16	J8, J9, J11 to J24	W HOLE			
13	1	J10	Dual-row header	40 pins		SAMTEC TSW-120-23-L-D
14	4	L1 to L3, L5	IND-COIL	1008CS	68 nH	Coilcraft 1008CS-680XGBB
15	2	L4, L6	IND-COIL	1008CS	82 nH	Coilcraft 1008CS-820XGBB
16	2	R1, R5, R6, R11 to R13	Resistor	1206	50 Ω	(49.9 Ω, 1%)
17	2	R2, R20	Resistor	1206	3900 Ω	
18	2	R3, R7	Resistor	1206	25 Ω	(24.9 Ω, 1%)
19	1	R4	Resistor	1206	1300 Ω	
20	1	R8	Resistor	1206	2000 Ω	
21	2	R9, R10	Resistor	1206	100 Ω	
22	4	R15 to R18	Resistor	1206	10 kΩ	
23	1	RP1	Resistor network	SIP-10P	10 kΩ	Bourns 4610X-101-103
24	1	TB1	Terminal block and pins	4-position		Wieland 25.602.2453.0 block Z5.530.3425.0 pins
25	1	U1	AD9852 or AD9854	LQFP-80		AD9852ASQ or AD9854ASQ
26	1	U2	74HC125	14 SOIC		SN74HC125D
27	1	U3	MC100LVEL16D	8 SOIC		MC100LVEL16D
28	4	U4 to U7	74HC14	14 SOIC		SN74HC14D
29	3	U8 to U10	74HC574	20 SOIC		SN74HC574DW
30	1	J11	36-pin connector			AMP 552742-1
31	6	W1 to W4, W8, W17	3-pin jumper			SAMTEC
32	10	W6, W7, W9 to W16	2-pin jumper			SAMTEC
33	2		Self-tapping screw	4–40, Philips, round head		
34	4		Rubber bumper	Square black		3M SJ-5018SPBL
35	1	AD9852/AD9854 PCB				GSO2669 Rev. E
36	2	R14, R19	0 Ω jumper	1206	0 Ω	
37	4		Pin socket			AMP 5-330808-6
38	1	Y1 (not supplied)	XTAL	COSC		(Not supplied)

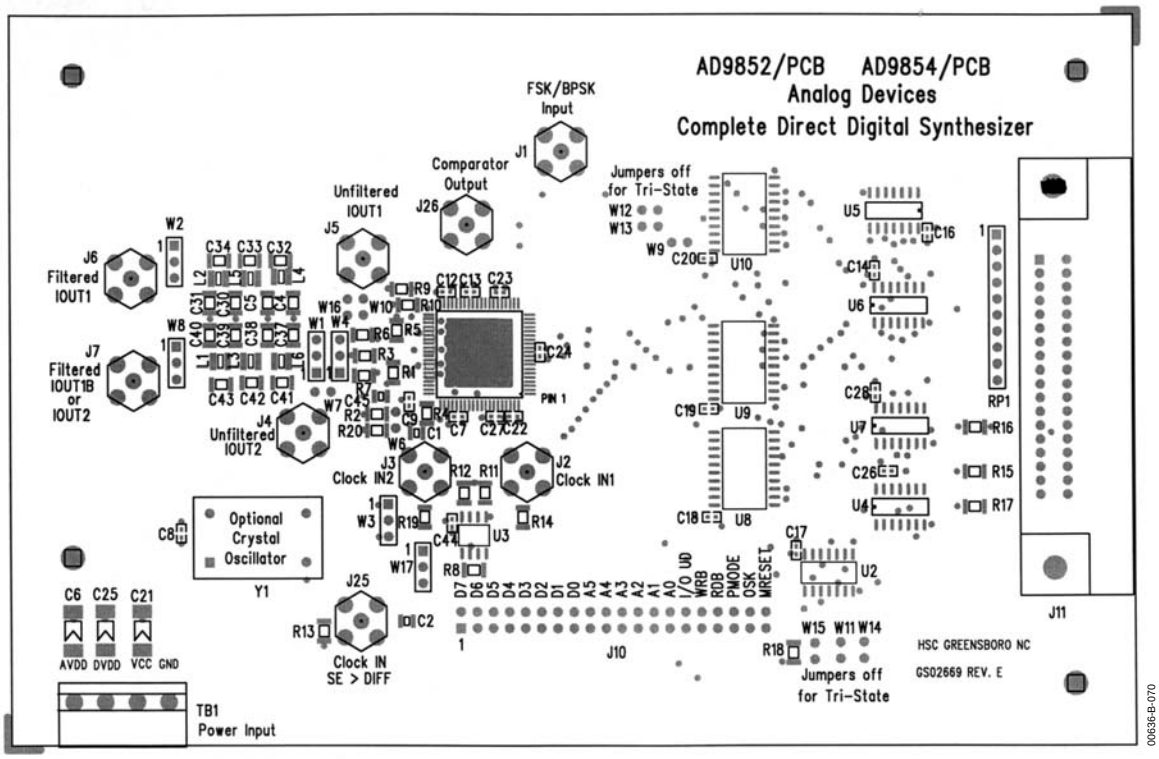

Figure 70. Assembly Drawing

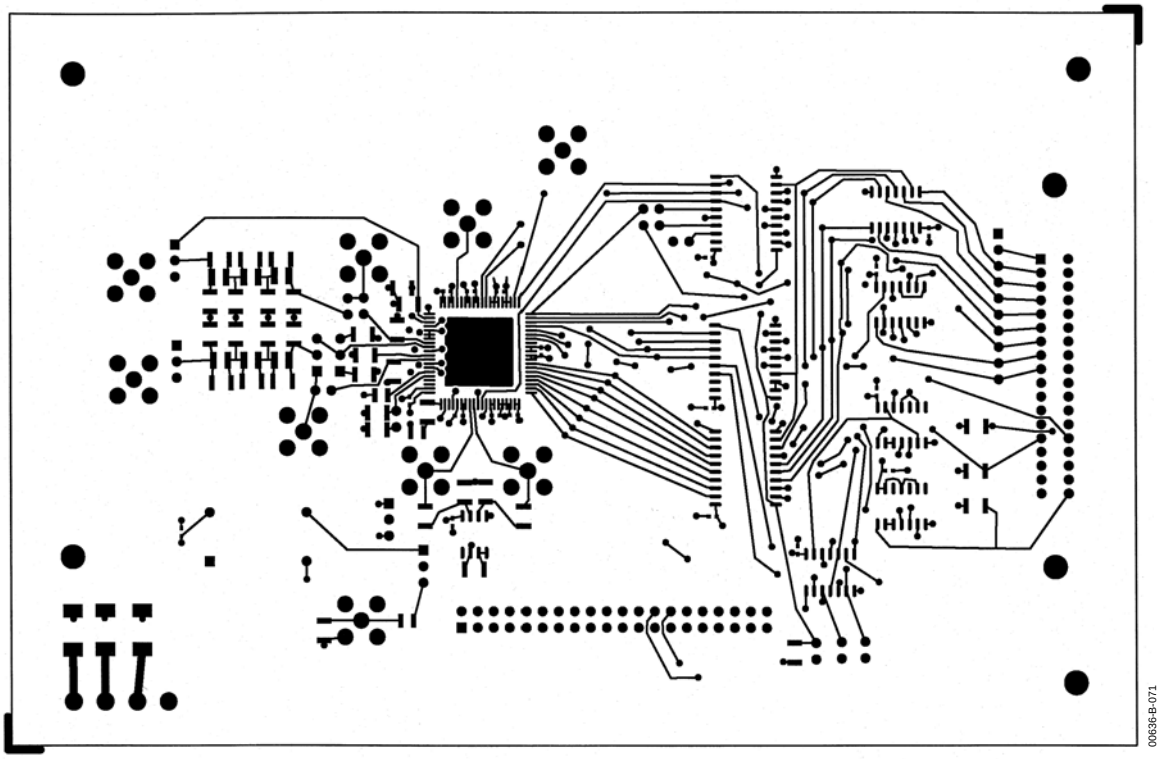

Figure 71. Top Routing Layer, Layer 1

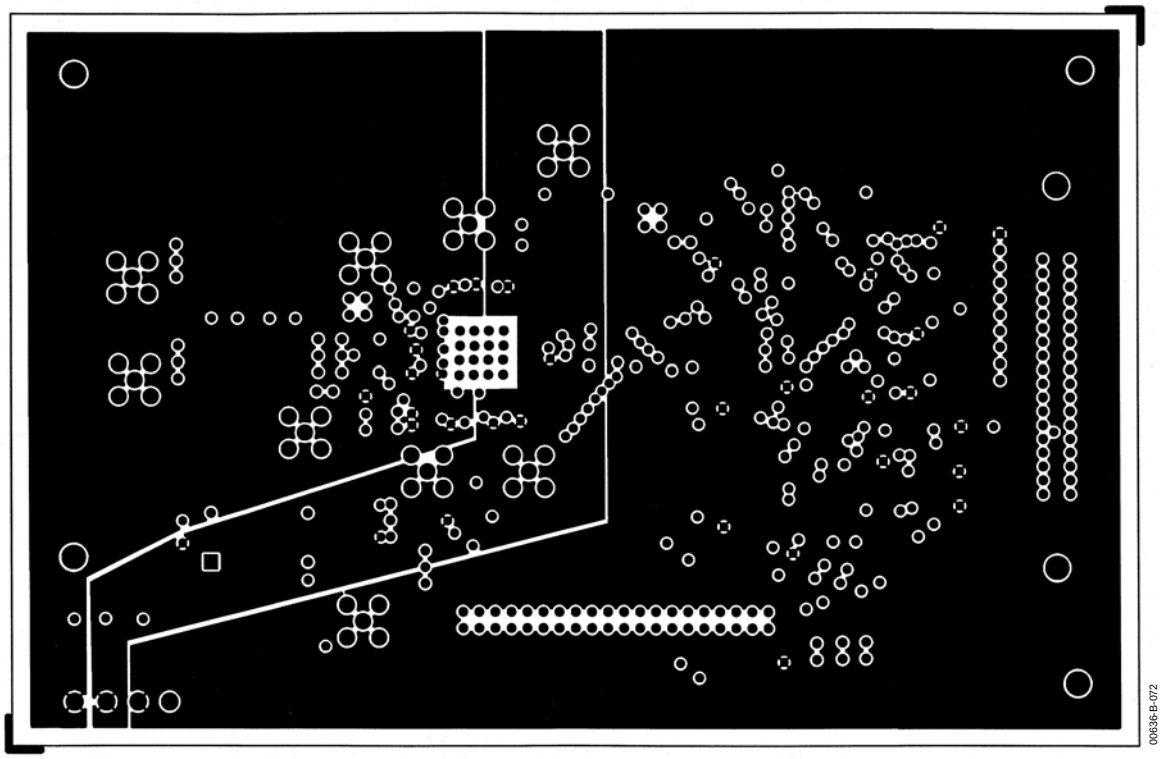

Figure 72. Power Plane Layer, Layer 3

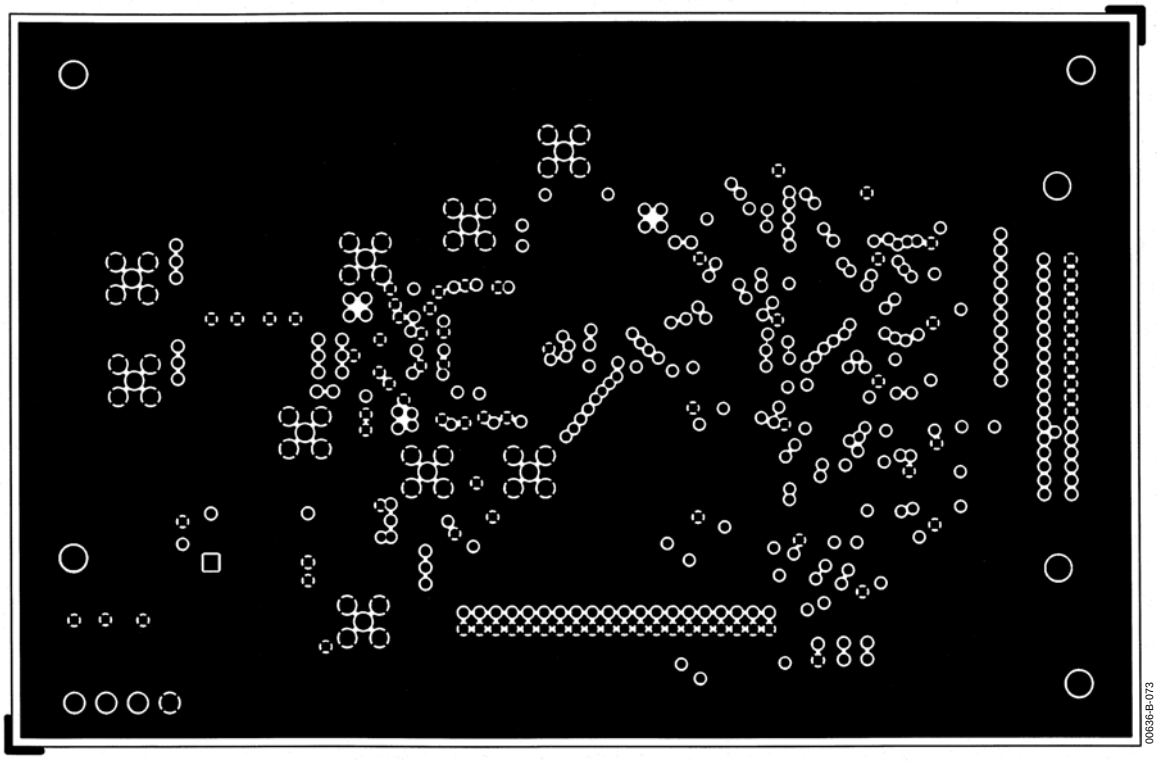

Figure 73. Ground Plane Layer, Layer 2

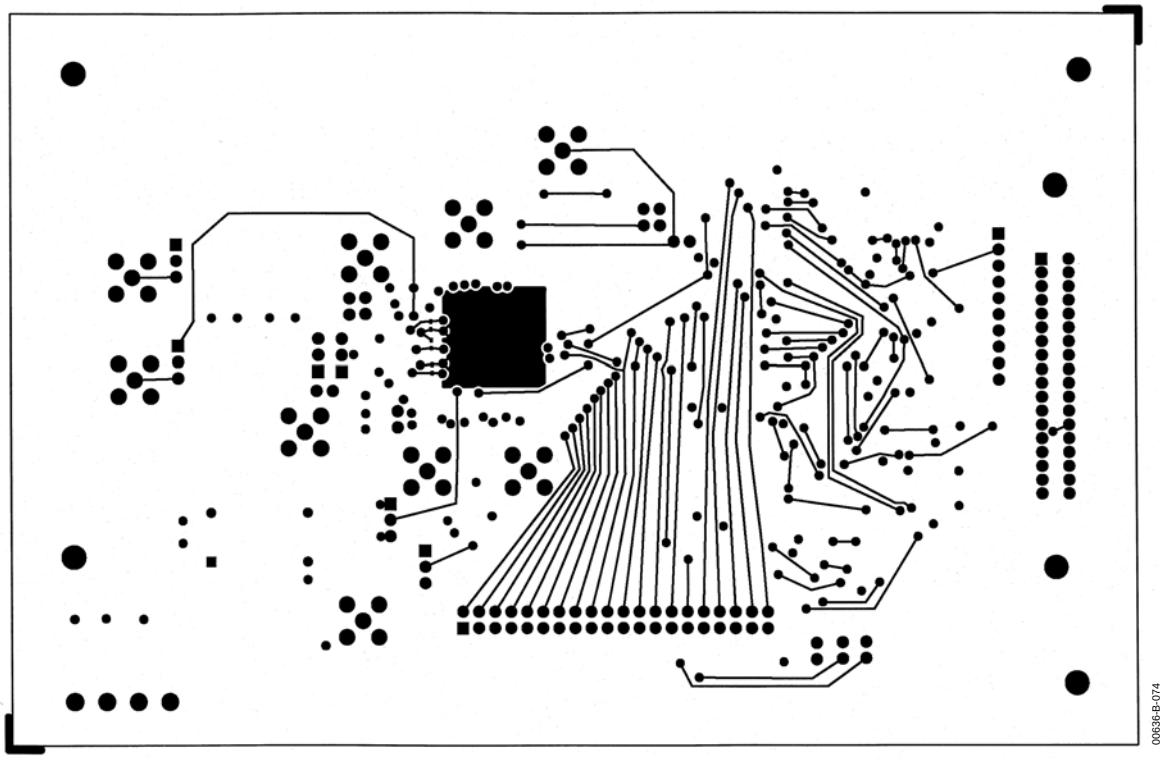

Figure 74. Bottom Routing Layer, Layer 4

OUTLINE DIMENSIONS

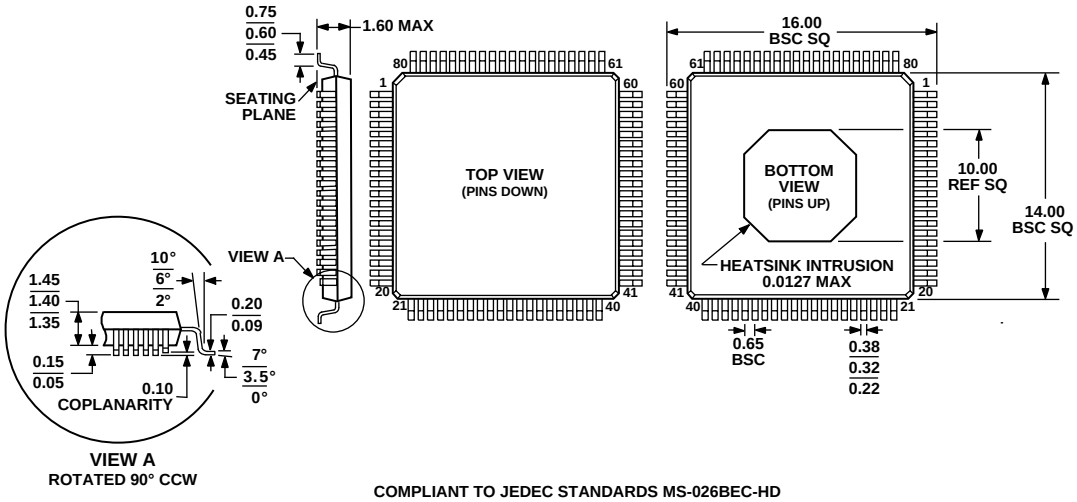

Figure 75. 80-Lead Low Profile Quad Flat Package, with Heatsink [LQFP_ED]
(SQ-80-2)
Dimensions shown in millimeters

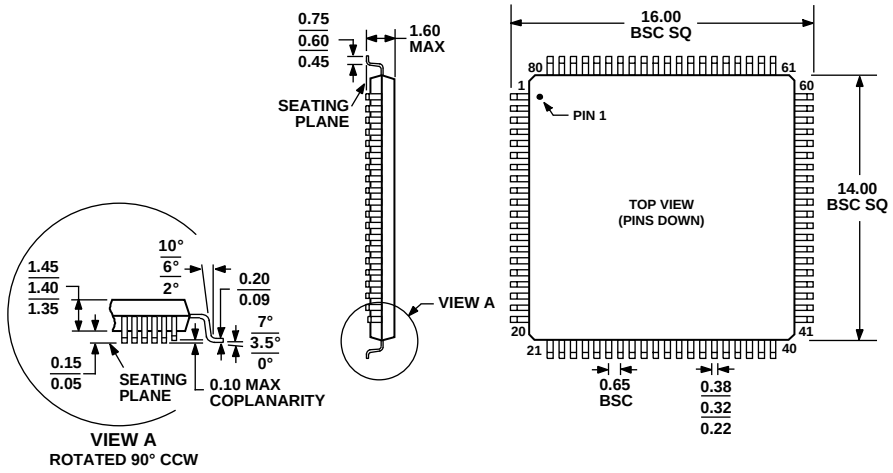

Figure 76. 80-Lead LQFP
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9854ASQ	–40°C to +85°C	Thermally Enhanced 80-Lead LQFP_ED	SQ-80-2
AD9854AST	–40°C to +85°C	80-Lead LQFP	ST-80-2
AD9854/PCB		Evaluation Board	

NOTES

C00636–0–10/04(C)